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Digitally programmable composite operational amplifier applications

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NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

DIGITALLY PROGRAMMABLE
COMPOSITE OPERATIONAL AMPLIFIER
APPLICATIONS

by

Ronald A. Crowell

September, 1993

Thesis Advisor:	Sherif Michael

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In this study, CMOS implementation of composite operational amplifiers onto a single chip is examined. Composite operational amplifiers are realized by interconnecting two or more single operational amplifiers in any one of four high performance circuit topologies. These high performance topologies result in composite operational amplifiers having useful bandwidths that are significantly larger than those associated with their constituent operational amplifiers without sacrificing closed loop gain. Computer simulations using PSPICE are compared with experimental results for performance evaluation. As an application a multiple feedback bandpass filter implementation is examined. This work successfully demonstates that composite topologies can satisfactorily implemented onto a single chip.

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Digitally Programmable
Composite Operational Amplifier
Applications

by

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Submitted in partial fulfillment
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ABSTRACT

In this study, CMOS implementation of composite operational amplifiers onto a single chip is examined. Composite operational amplifiers are realized by interconnecting two or more single operational amplifiers in any one of four high performance circuit topologies. These high performance topologies result in composite operational amplifiers having useful bandwidths that are significantly larger than those associated with their constituent operational amplifiers without sacrificing closed loop gain. Computer simulations using PSPICE are compared with experimental results for performance evaluation. As an application, a multiple feedback bandpass filter implementation is examined. This work successfully demonstrates that composite topologies can satisfactorily implemented onto a single chip.

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I. INTRODUCTION

A. PROBLEM

Operational amplifier or "op amp" is the term used to describe an electronic device with a wide variety of linear applications. Introduced in 1948 as a single vacuum tube device, the op amp has evolved from a device used to fashion circuits to perform analog computing operations to today's transistorized devices with applications in such diverse fields as communications, automotive instrumentation, and sonar as well as a host of others. Despite its popularity and versatility, the single op amp has frequency limitations that ultimately restrict the range of operating frequencies for linear active circuit applications. These limitations have been addressed through the development and testing of a new variety of op amps known as composite op amps. This new variety of op amp, in simple terms, is a collection of two or more single op amps connected in such a way so as to realize a mixed or composite op amp possessing a larger useful bandwidth than either of the constituent op amps. The theory concerning the implementation of composite op amps has been thoroughly examined in technical literature and verified through the construction and testing of working models using discrete components. The purpose of this study is to verify

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whether or not composite op amps can be satisfactoïily implemented on a chip, namely the MLA-6018. The MLA-6018, which is the culmination of the work outlined in reference 1, is a semi-custom designed chip with three composite op amp topologies that incorporate CMOS Field Effect Transistor (FET) technology.

The successful development of composite op amp chip technology will combine a broadened range of useful linear active circuit operating frequencies with the simplicity and reliability of the op amp. Among the beneficiaries of this technology would be improved military communications systems as well as signal processing systems.

B. APPROACH

The MLA-6018 is examined by first conducting computer simulations to provide baseline data for later comparisons. The chip manufacturing process is verified by means of an operability test where the chip is checked to see if all incorporated composites will operate. After operability is verified, composite performance evaluation is conducted and the results are compared against the baseline data obtained from the computer simulations and the experimental data from reference 1. Finally, a multiple feedback bandpass filter application for the MLA-6018 is examined in much the same manner as the chip itself.

C. SCOPE

This study is divided into seven chapters. Chapter I, the introduction, offers the reader brief overviews of the history of op amps and the approach used in this study.

Chapter II provides detailed discussions of ideal and non-ideal characteristics for single and composite op amps. Problem areas and their solutions are also addressed.

The design of the MLA-6018 chip is addressed in Chapter III. The discussion includes the descriptions of the workings of the internal op amps and compensating resistance networks, overviews of the implementation of composite topologies, and the fabrication process for the chip.

Chapter IV contains the results of using PSPICE models to obtain performance data from computer simulations of the composites built onto the MLA-6018. Here, stimuli are varied and the composite's responses are reported.

Chapter V involves the testing process discussed earlier. It also provides comparison with the baseline performance data obtained in Chapter IV.

Chapter VI is the applications chapter. A multiple feedback bandpass filter is postulated, simulated, experimentally tested, and evaluated.

Chapter VII summarizes the previous chapters, while at the same time offering recommendations for future uses and modifications for the MLA-6018.

An appendix containing PSPICE code lists is provided as reference material for the reader who is interested in working with the composite op amp models used in this study.

II. SINGLE VERSUS COMPOSITE OPERATIONAL AMPLIFIERS

A. SINGLE OPERATIONAL AMPLIFIERS

A single or conventional linear circuit op amp may be generally described as a direct-coupled high-gain amplifier that uses feedback to control its performance characteristics [Ref. 2]. Ideally an op amp has constant gain over all frequencies or an infinite Gain Bandwidth Product (GBWP), infinite common-mode rejection ratio (CMRR), infinite input impedance, zero output impedance, and an infinite open loop gain. The properties of the ideal op amp in the open loop configuration seemingly preclude its use in any practical application. Using feedback to place the op amp in a closed loop configuration, however, allows for practical use of the op amp.

In practice, an op amp performs non-ideally. The open loop gain is not only finite, but also decreases as frequency increases. The potential exists for the op amp to oscillate as the frequency increases. It is possible for conditions to exist such that, at the point where the op amp frequency response falls to unity gain, a phase margin magnitude in excess of 180° would result in the amplifier entering an unstable oscillation. This can be corrected through the use of

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frequency compensation, which will be discussed in more detail later.

CMRR is expressed by

$$CMRR = 20 Log_{10} \frac{|A|}{|A_{cm}|} \qquad (2.1)$$

where $|A|$ is the differential gain and $|A_{cm}|$ is the common gain. If $|A_{cm}|$ is zero, then equation (2.1) yields an infinite CMRR. An infinite CMRR implies that the op amp should produce a zero output for an input common to both input terminals (common-mode). The non-ideal op amp has a finite CMRR that is a function of frequency, decreasing as frequency increases. Differences between transistors in the differential input stage (which are discussed later) give rise to the finite CMRR. When the op amp is an inverting configuration, the effect of a finite CMRR is negligible because the non-inverting terminal is grounded. When however, the op amp is placed in a non-inverting or differential input configuration and high accuracy is required, the effect of a finite CMRR is no longer negligible and must be taken into account [Ref. 3]. Thus the non-ideal op amp produces a non-zero output in response to a common-mode input.

The output impedance for the non-ideal op amp is not zero, but is generally so small that it may be considered to be zero without incurring significant error in circuit calculations.

Similarly, the input impedance is not infinite, but is very large.

Because the op amp is directly coupled, it is susceptible to dc problems [Ref. 3]. The first problem involves the input offset voltage (V_{os}). In a practical op amp, it is not possible to manufacture exactly identical transistor pairs for the differential input stage, thus electrical characteristic differences or mismatches between transistor pairs result. These mismatches give rise to V_{os}. Since the nature of the component mismatches that result in V_{os} is somewhat random and cannot be known prior to manufacture, V_{os} can have a range of magnitudes and either positive or negative polarity. The effect of V_{os} is manifested in an erroneous signal output consisting of true signal superimposed on a dc error signal. Using the inverting configuration shown in Figure 2.1, the magnitude of this error signal is given by

$$V_o = V_{os} [1 + \frac{R_2}{R_1}]$$
(2.2)

For example, if a non-inverting op amp with a closed loop gain of 100 has V_{os} = 3 mV, then the dc output voltage would be valued ± 0.3 volts. Any subsequent input signal would then be superimposed on this 0.3 volt dc signal and thus be erroneous. For op amps using bipolar junction transistors, V_{os} is about 1 to 5 mV, while for CMOS op amps, V_{os} may vary from a few to as

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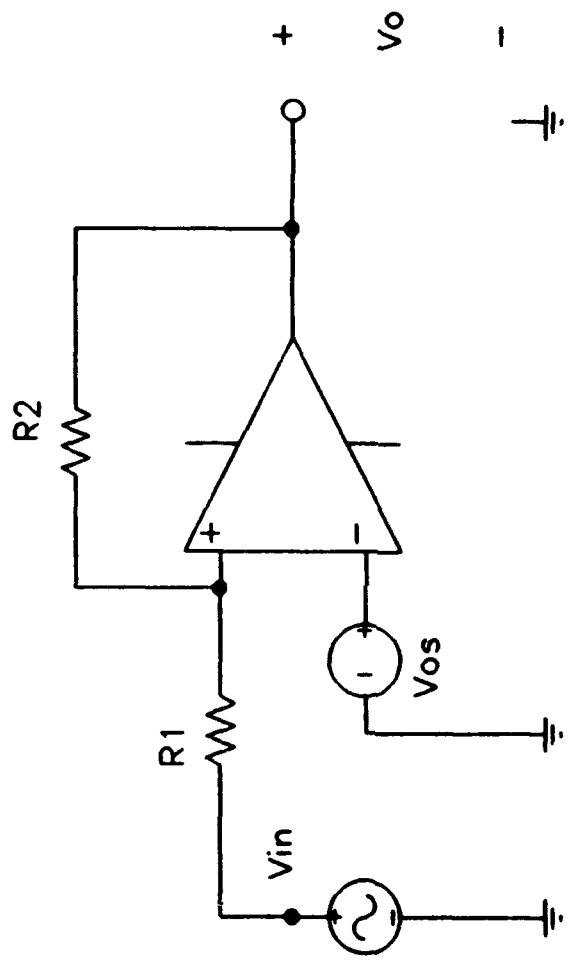
Figure 2.1   Example of Circuit For Measuring V_os

many as 25 mV [Refs. 3,4]. A second dc problem is input current offset (I_{os}). Since the transistors paired in the differential input stage are not exactly identical, it follows that each requires a different input bias current for proper operation. The magnitude of that difference is called I_{os}. The effect of I_{os} is to produce a very small dc output voltage. For op amps using bipolar junction transistors, I_{os} tends to be on the order of tens of nanoamperes and picoamperes for CMOS op amps. The dc voltage output due to input bias currents is approximately the sum of the input bias currents of the differential input stage transistors multiplied by the magnitude of the feedback impedance [Refs. 3,4].

Frequency compensation involves incorporating an internal frequency compensation capacitor in order to ensure amplifier stability for a particular range of closed loop gain values at high frequencies. It is accomplished by reducing the op amp gain as frequency increases. Without frequency compensation, the gain and phase shift could be large enough at a certain high frequency that there would be sufficient output fed back to the input to produce oscillations. The price of improved stability, however, is reduced small-signal bandwidth, low slew rate, and reduced power-bandwidth. [Ref. 5]

The net effect of the parameters in the foregoing discussion is to reduce the useful bandwidth of the op amp.

This is not a significant concern unless high frequency applications are required.

B. COMPOSITE OPERATIONAL AMPLIFIERS

A composite op amp, as its name implies, is an op amp topology obtained from the combination of at least two other op amps. Generally, the composite op amp offers an improvement over single or conventional op amp performance in terms of extended useful bandwidth, low sensitivity to component and op amp mismatch, and wide dynamic range. [Ref. 6]

References 1 and 2 provide detailed discussions regarding the generation of composite op amp topologies. Of the 136 possible composite configurations using two op amps (C2OA's), four were found to offer superior performance in the areas previously discussed. Of the four superior performing composites, three are contained in the MLA-6018 and are shown in Figure 2.2.

A discussion of C2OA bandwidth performance must be approached from the standpoint of stability. The op amps internal to the C2OA are each frequency compensated using frequency compensation capacitors. This compensation technique, however, is not sufficient to guarantee the stability of the C2OA. The resistance networks for the C2OA's shown in Figure 2.2 are referred to as "internal compensation resistance networks", where A (also known as α) is a real number used as a multiplier. It is the selection of this

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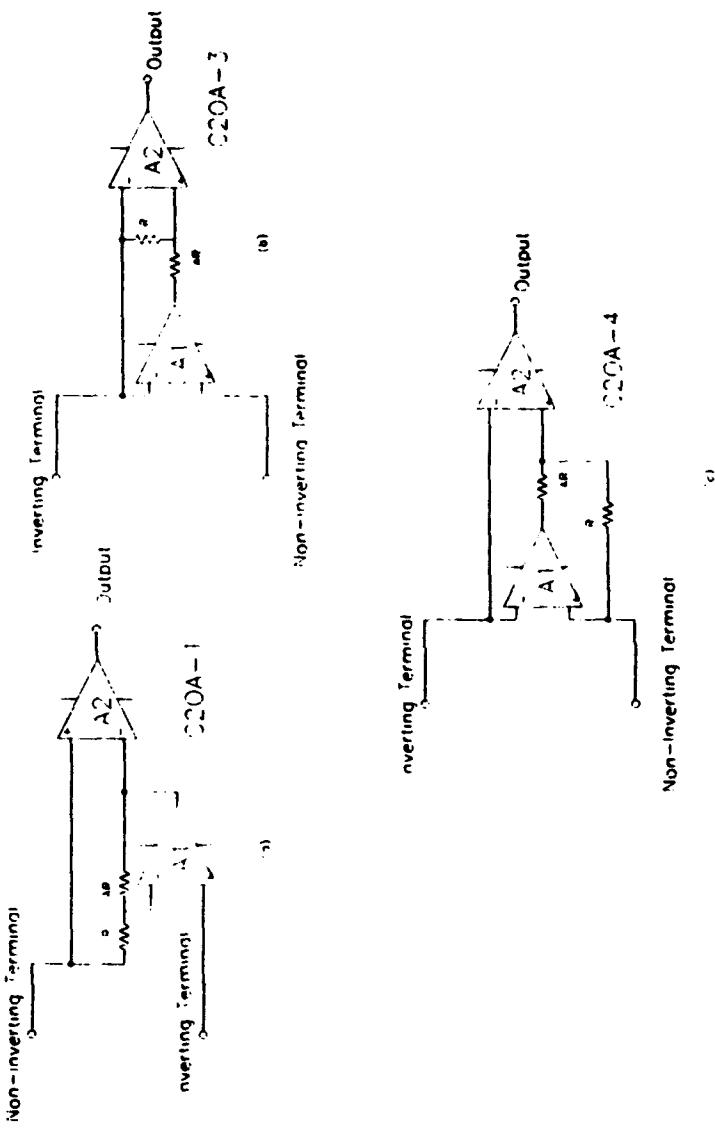
Figure 2.2   Composite Topologies Within the MLA-6018

multiplier value, coupled with the desired finite gain k, that will ultimately determine the stability of the composite. By applying the Routh-Hurwitz stability criterion [Ref. 6], the necessary and sufficient conditions for stability have been found to be

$$(1+\alpha) < \frac{(1+k)}{2} \tag{2.3}$$

for the C2OA-1,

$$(1+\alpha) > \sqrt{(1+k)} \tag{2.4}$$

for the C2OA-3, and

$$(1+\alpha) > 4(1+k) \tag{2.5}$$

for the C2OA-4.

The appropriate selection of α and k are guided by the following equations for Q_p the response quality factor:

$$Q_p = \frac{(1+\alpha)}{\sqrt{1+k}} \sqrt{\frac{\omega_2}{\omega_1}} \tag{2.6}$$

for the C2OA-1,

$$Q_p = \sqrt{\frac{(1+k)(1+\alpha)\omega_1}{\omega_2}} \tag{2.7}$$

for the C2OA-3, and

$$Q_p = \sqrt{\frac{(1+k)\omega_1}{(1+\alpha)\omega_2}} \tag{2.8}$$

for the C2OA-4.

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Here ω_1 and ω_2 are the unity gain bandwidths (expressed in radians) of the A1 and A2 position op amps, respectively. Once Q_p, k, and α are selected, the bandwidth performance of the C2OA can be estimated as

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1+k}} \qquad (2.9)$$

or

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1+k)(1+\alpha)}} \qquad (2.10)$$

For the C2OA-1, the 3-dB bandwidth, ω_p, is found from equation (2.9), while the 3-dB bandwidths of the C2OA-3 and C2OA-4 are found from equation (2.10). The result is a composite that yields a significant improvement in useful bandwidth over that for a single op amp (Figures 2.3 through 2.5).

CMRR for the composite op amp, as in the case of the single op amp, is not infinite. For the C2OA-1 and C2OA-3, CMRR has a value of $A_{o1}+1/2$, and that for the C2OA-4 is $A_{o1}+\alpha+1/2$. (A_{o1} is the open loop gain of the A1 position amplifier.) CMRR becomes negligible under the same conditions as for the single op amp.

Input and output impedance performance for the composite op amp is similar to that for the single op amp. Input impedances are finite but very large, while output impedances

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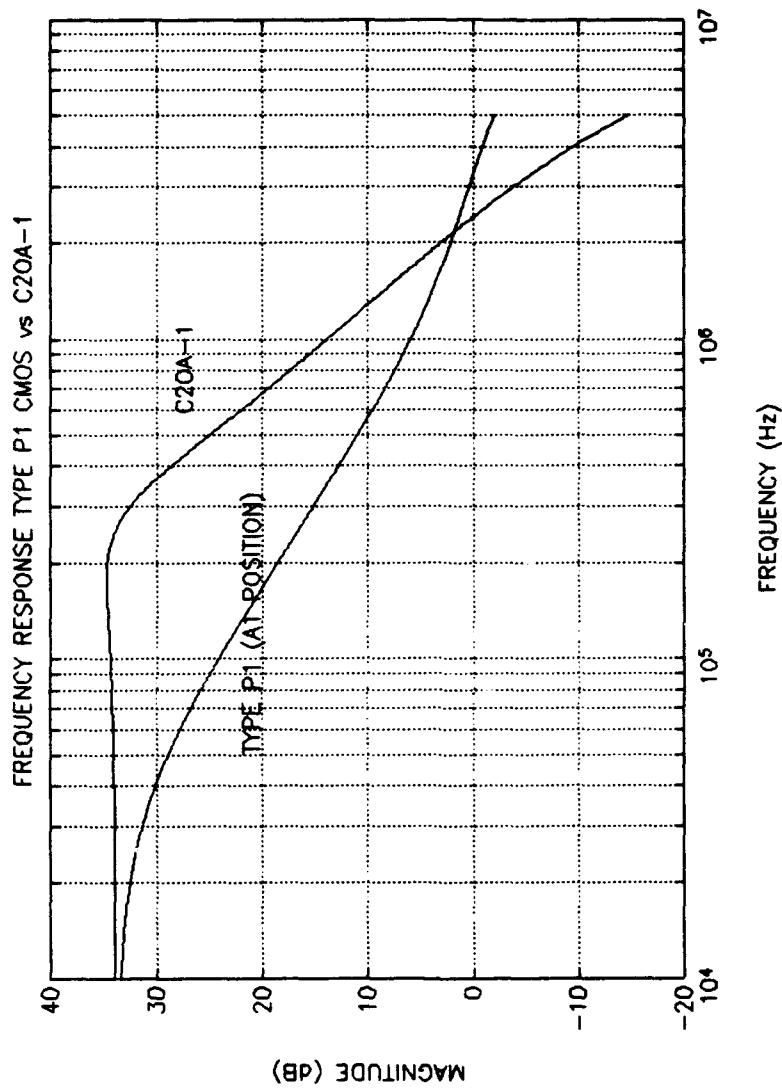
Figure 2.3   Comparison of C20A-1 vs Single Type P1 Op Amp Frequency Response

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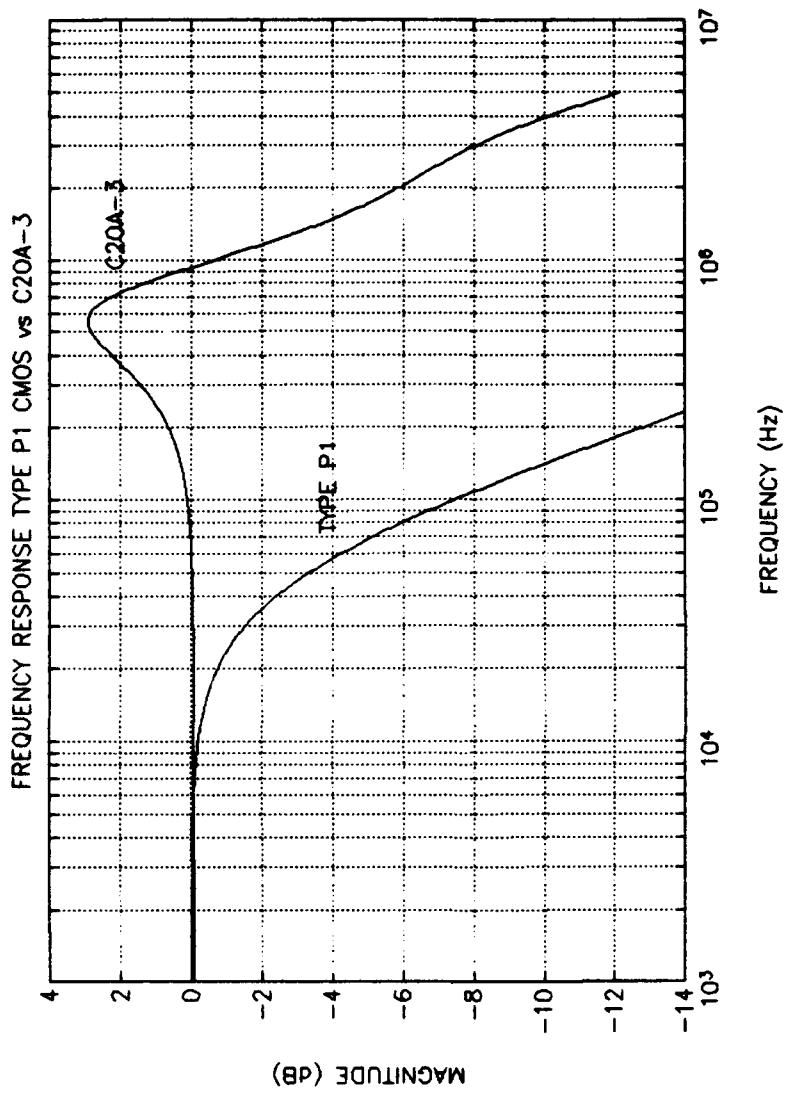
Figure 2.4   Comparison of C20A-3 vs Single Type P1 Op Amp Frequency Response

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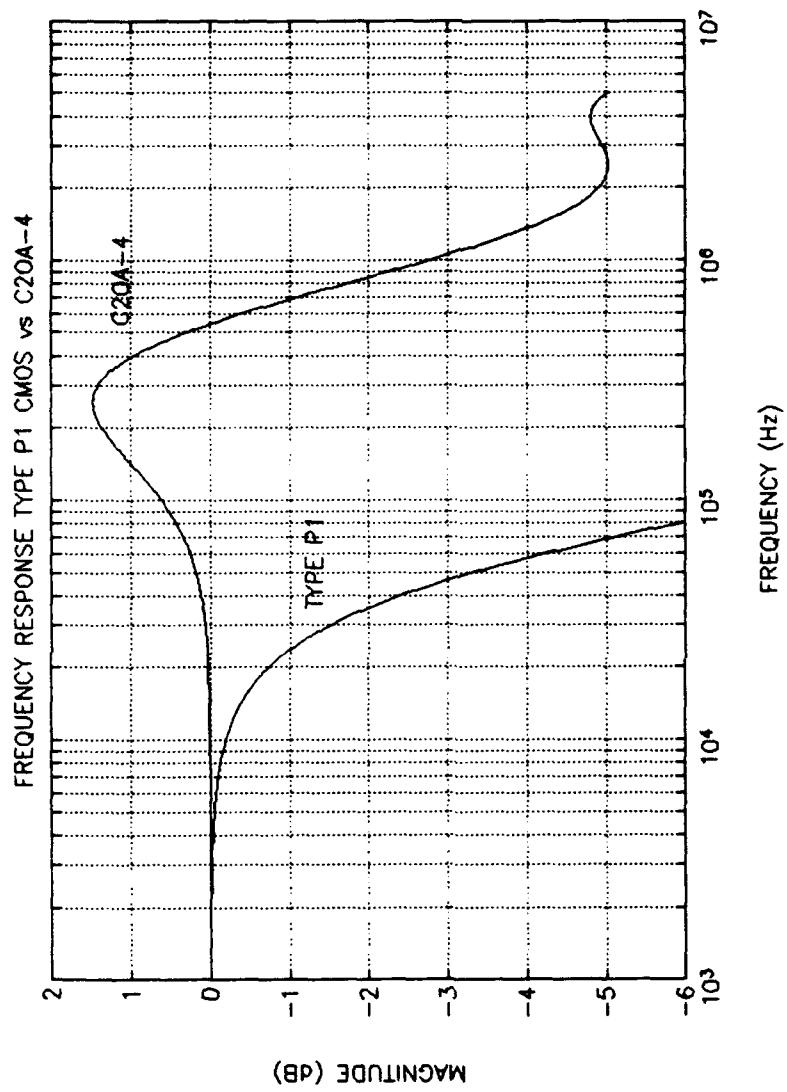
Figure 2.5 Comparison of C20A-4 vs Single Type P1 Op Amp Frequency Response

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are very small, but non-zero.

It might be reasonable to expect amplified V_{os} in the performance of the composite op amp, but that is an unfounded expectation. It has been found that the A2 position amplifier's contribution to the overall V_{os} is just $V_{os(A2)}$ divided by A_{o1}. Since the open loop gain for the A1 position amplifier is several orders of magnitude larger than $V_{os(A2)}$, the offset contribution from the A2 position amplifier is reduced to insignificance [Ref. 1]. This means that the overall V_{os} is ostensibly due to $V_{os(A1)}$.

Input offset current has no measurable effect on composite op amp performance.

C. SUMMARY

The composite op amp offers improved bandwidth performance over that of a single op amp, while suffering no degradation in dc performance. Frequency compensation for the composite is slightly more involved than for the single op amp. The designer must not only ensure that each internal op amp is internally compensated, but also must evaluate composite topology, circuit gain, and internal compensation resistance. Non-ideal performance characteristics do not differ significantly between the two types of op amps discussed above. Hence, the composite offers more advantages than disadvantages in terms of utility.

III. MLA - 6018 CHIP DESIGN

A. BASIC CONCEPT

The MLA-6018 is a 24 pin dual-in-line ceramic package featuring CMOS implementation of three programmable composite amplifiers on a single chip. Based on design parameters supplied from reference 1, the MLA-6018 was produced in 1986 by Ferranti Interdesign using what was termed a CMOS Monochip. A Monochip is a predesigned and preprocessed array of circuit elements ready to be interconnected into a custom integrated circuit for a special requirement [Ref. 4]. This is referred to as semi-custom design process which allows the designer to simply interconnect the required components in order to achieve a design objective. While simple, the semicustom design process does not allow interconnections for extremely complex circuitry as would be found on a full production chip. The MLA-6018, however, is not a full production chip and was not designed for any purpose other than the study of composite op amps. Thirty chips have been manufactured providing a large enough sample to fairly evaluate the ability to satisfactorily implement composite amplifiers in CMOS integrated circuit form and provide a test platform for the study of composite amplifier applications.

B. DESIGN PARAMETERS

1. The General Op Amp

A P-channel-input two-stage CMOS operational amplifier (Type P-1) [Ref. 4] with a high impedance output stage (Figure 3.1) is the basic component from which the composite forms C2OA-1, C2OA-3, and C2OA-4 are generated. The MLA-6018 version of this op amp employs n-channel and p-channel transistors with respective W/L ratios of 24/12 and 60/12. The first stage of the Type P-1 "quades" or parallels a pair of transistors for each transistor in the differential input pair Q101, Q102 and the current mirror Q105, Q106. This has the effect of cancelling threshold voltage mismatching between the input stage transistors and the input offset voltage (V_{os}). Ultimately, this results in the overall V_{os} for the composite being approximately that of the internal amplfier in the A1 position [Ref. 1]. Q105 provides stage biasing through the current mirror and is biased through a single biasing pin that may be connected to an external resistance. Transistors Q1 and Q2 are active current mirror loads for the differential input pair.

The second stage of the P-1 is driven differentially at the gates of Q3 and Q4. Q4 is triply "quaded" to help reduce the output impedance of the op amp. The current mirror (Q103 and Q104) is identical in construction to the Q105 and Q106 current mirror, duplicating the operating current for Q3
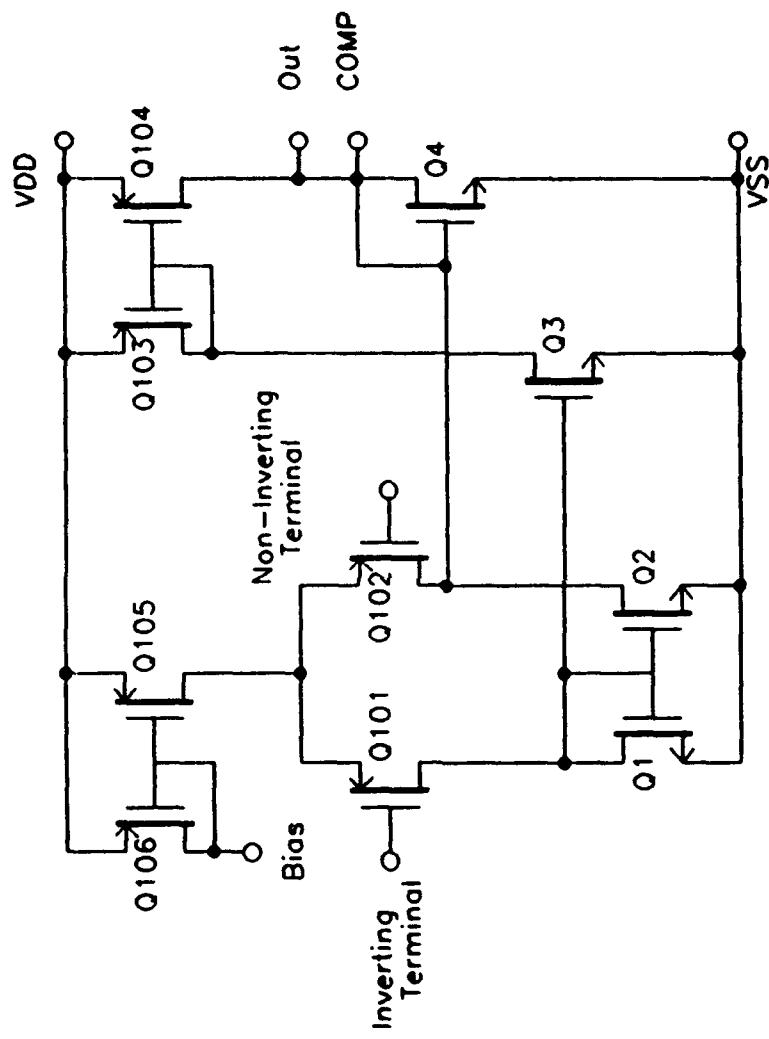
Figure 3.1 Ferranti Interdesign Type P1 CMOS Op Amp

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and thus providing an active load for the output transistor Q4 [Ref. 4].

The A2 position amplifier features triply quaded p- and n-channel transistors with respective W/L ratios of 290/24 and 155/24 at the output node. This increases the output current available and effectively reduces the output resistance. This technique is used in the C2OA-1 structure but, due to space and routing limitations, is not used to the same degree in neither the C2OA-3 nor C2OA-4 structures. This issue will be addressed later.

2. Compensating Resistance

The compensating resistance on the MLA-6018 is achieved through the use of a selectable resistance network. Switching is performed by a series of CMOS transmission gates. By applying the logic signals from Table I, the user may select resistances that are integer multiples of 12.5 kΩ, where the integer values (α) range from one to eleven.

Varying this compensating resistance has the effect of varying α and thus, in turn varying Q for the frequency response. Four pins are provided for this purpose.

3. Composite Generation

a. C2OA-1

The C2OA-1 structure (Figure 3.2) is implemented as a single operational amplifier with separate inverting and non-inverting inputs, a single output, four switching lines

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TABLE 1
LOGIC TABLE FOR PROGRAMMING α ON THE MLA-6018

C2OA-N PROGRAMMING TABLE			
α	PIN 8(4)	PIN 9(5)	PIN 10(6)	PIN 11(7)
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	1	0	0
9	1	1	0	1
10	1	1	1	0
11	1	1	1	1

NOTE: Pins 8 through 11 are used for C2OA-1; Pins 4 through 7 are used for C2OA-3/4.

R10 = 12.5K
R9 = 50K
R8 = 50K
R7 = 25K
R6 = 12.5K

Cc = 10pF
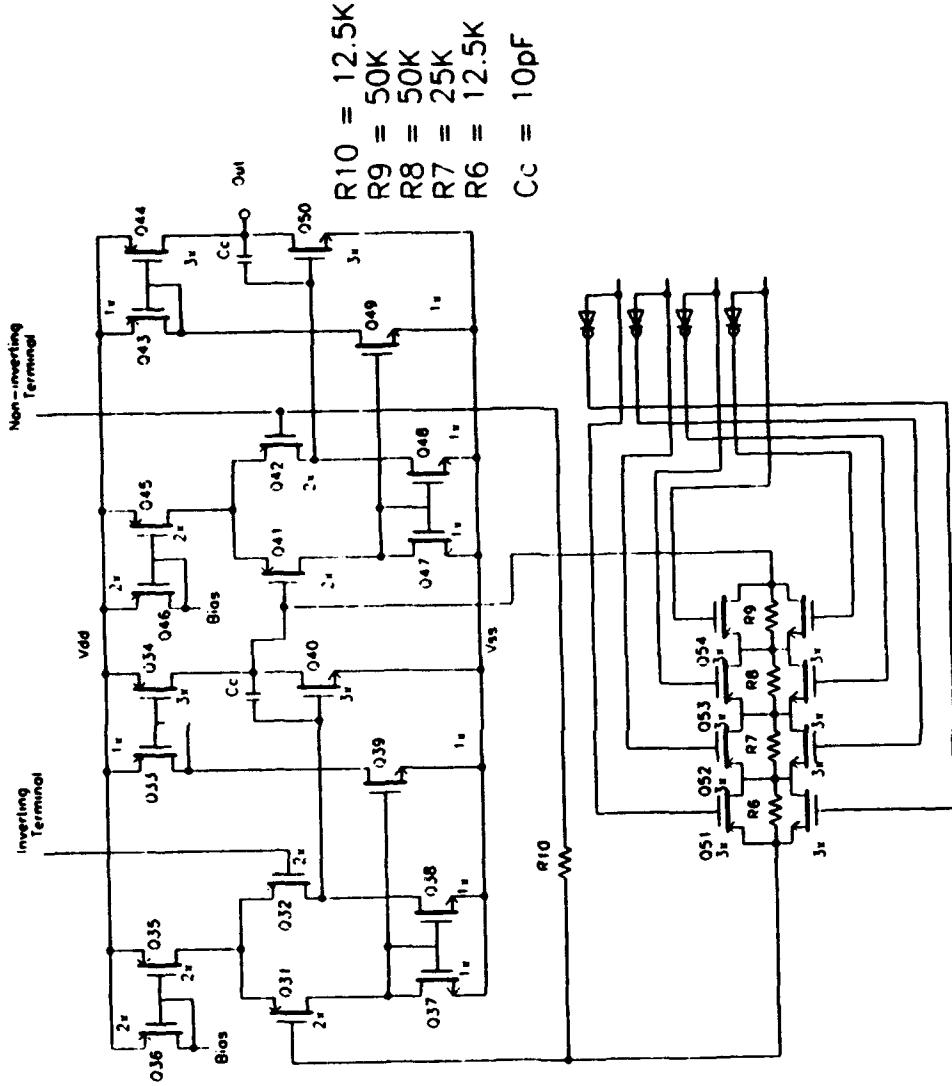
C20A-1 CMOS OP-AMP

Figure 3.2   Schematic For C20A-1

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for selecting or "programming" the value of the compensating resistance, and a pair of biasing terminals (one for each internal op amp). The biasing pins allow for connection of an external resistance which is used to adjust the DC bias current which, in turn, affects slew rate and open loop gain. Since the output from the A1 position amplifier is smaller than that for A2 position amplifier, there is a potential for poor full-power bandwidth performance in the composite. To illustrate this problem, consider the following equation:

$$f_M = \frac{SR}{2\pi V_{omax}} \qquad (3.1)$$

where f_M is the full-power bandwidth, SR is the slew rate, and V_{omax} represents the amplifier rated output voltage. If the A1 and A2 position amplifiers have the same slew rate and the A2 output voltage is greater than the A1 output voltage, then it follows from equation 3.1 that $f_{M(A2)}$ will be smaller than $f_{M(A1)}$. This is an unacceptable condition. Ideally, the bias should be adjusted such that the slew rate for the A2 position op amp is higher than that for the A1 position op amp thus improving the full power bandwidth of the composite [Ref. 1].

b. *C20A-3 and C20A-4*

Figure 3.3 shows the MLA-6018 C20A-3 and C20A-4 amplifiers are implemented as one structure. This structure is equipped with terminals in the same fashion as the C20A-1

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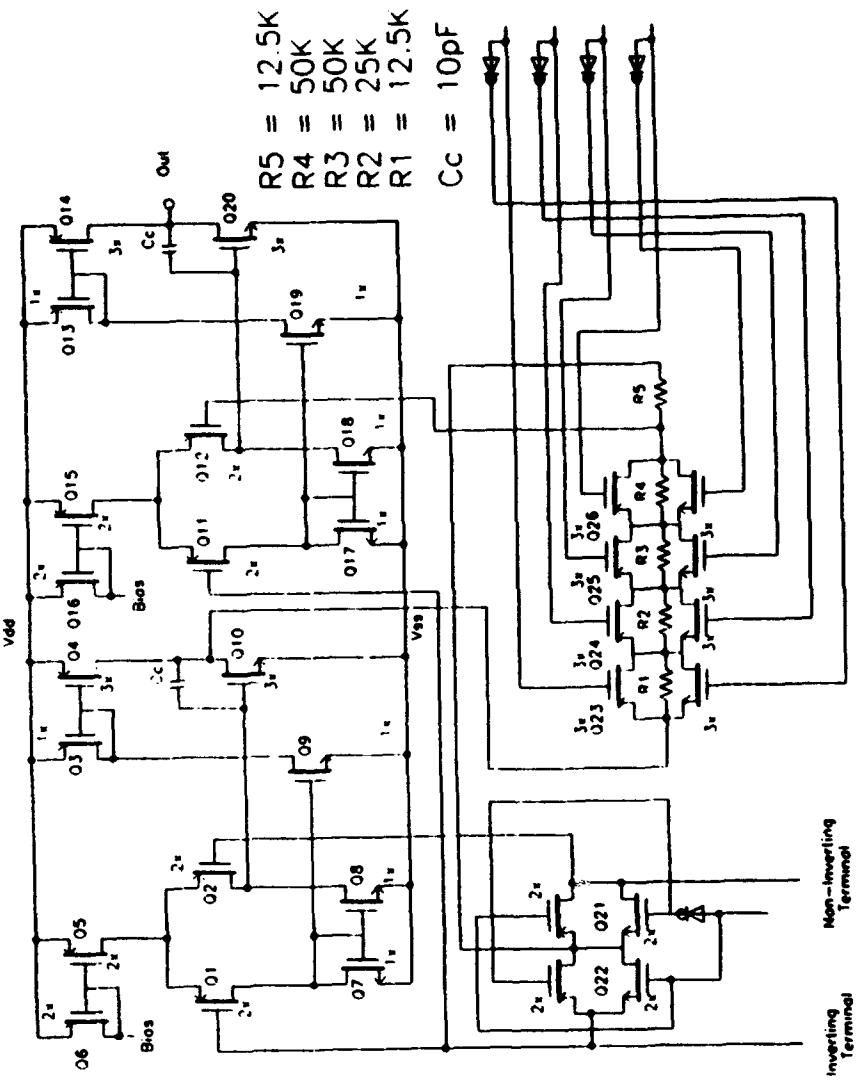
Figure 3.3 Schematic For C20A-3/4

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structure, but with one additional pin. The additional pin, pin 3, provides a logical input to a set of CMOS transmission gates that are used to select either the C2OA-3 or C2OA-4 amplifier. A logical "0" placed on pin 3 selects the C2OA-3 amplifier, while a logical "1" selects the C2OA-4 amplifier. Besides differing from the C2OA-1 in terms of topology, the C2OA-3/4 structure, due to MLA space and routing limitations, does not use exactly the same A2 position amplifier as the C2OA-1. Instead, the A2 position amplifier is identical to the A1 position amplifier. In this instance, biasing becomes extremely critical to proper operation.

C. FABRICATION

The MLA-6018 is fabricated using metal gate CMOS technology. In the first manufacturing step, an initial oxide layer is grown over a silicon wafer. Next, after applying a photosensitive layer to the top of the wafer, a photomask is used to etch the circuit patterns onto the wafer. Subsequent photomask applications are then used to separately define the PMOS and NMOS transistors, transistor active gate areas, electrical contact points, and lastly, provide a layer of protective glass over the entire top surface of the wafer. After electrical testing, the wafer is optically inspected, and then assembled in a ceramic package [Ref. 4]. The finished circuit and pin layouts are shown as Figures 3.4 and 3.5.
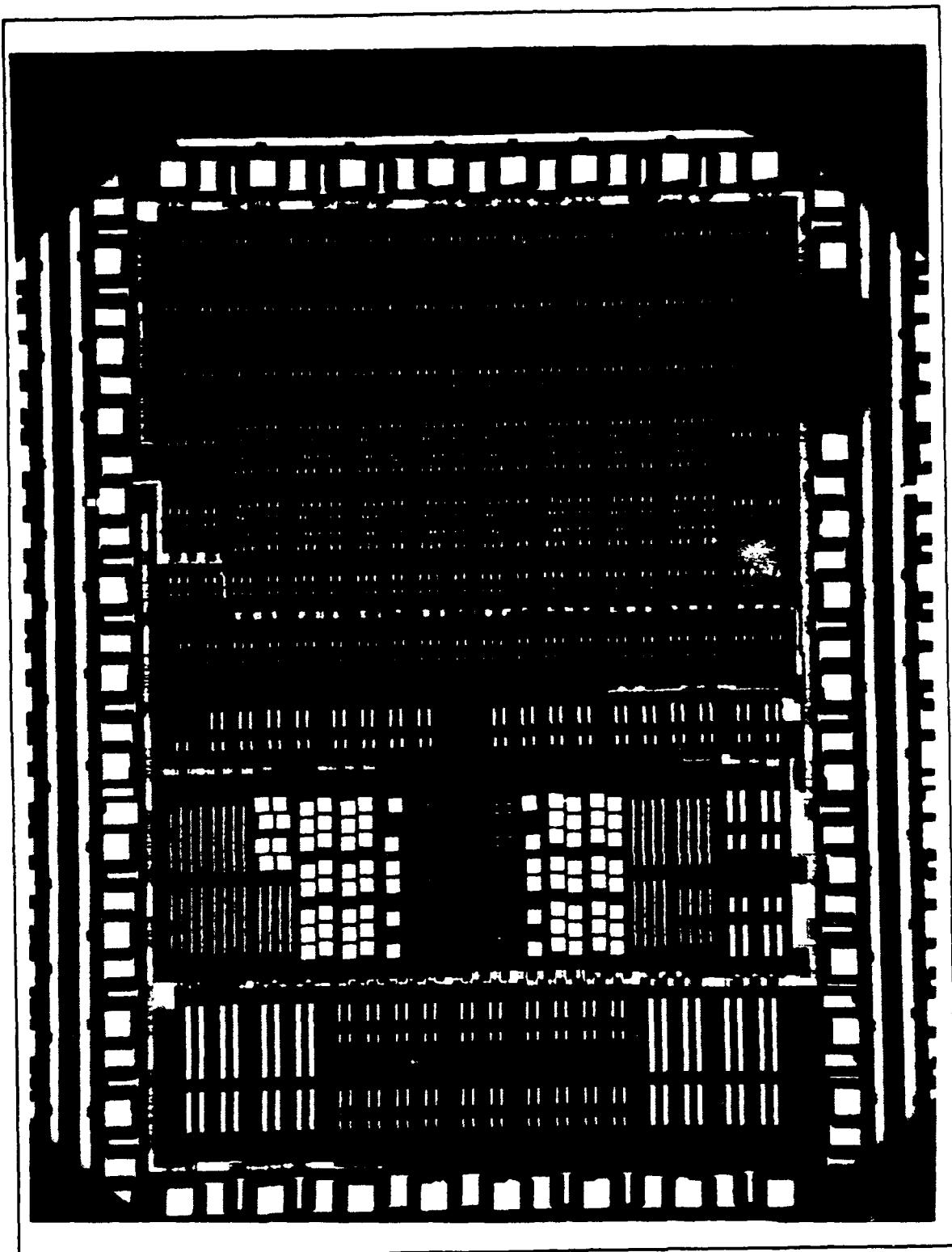
Figure 3.4   Fabricated Layout of the MLA-6018

```
VOUT  C2OA-3/4  ————  | 1           24 |  ————  VSS

BIAS-C2OA3/4  (A2)  ————  | 2           23 |  NC

                    ————  | 3           22 |  NC

                    ————  | 4           21 |  NC

                    ————  | 5           20 |  ————  BIAS-C2OA-1 (A2)

                    ————  | 6           19 |  ————  ( - ) C2OA-1

                    ————  | 7           18 |  ————  (+) C2OA-1

                    ————  | 8           17 |  ————  BIAS-C2OA-1 (A1)

                    ————  | 9           16 |  ————  VOUT  C2OA-1

                    ————  | 10          15 |  ————  (+) C2OA-3/4

                    ————  | 11          14 |  ————  ( - ) C2OA-3/4

           VDD  ————  | 12          13 |  ————  BIAS-C2OA-3/4 (A1)
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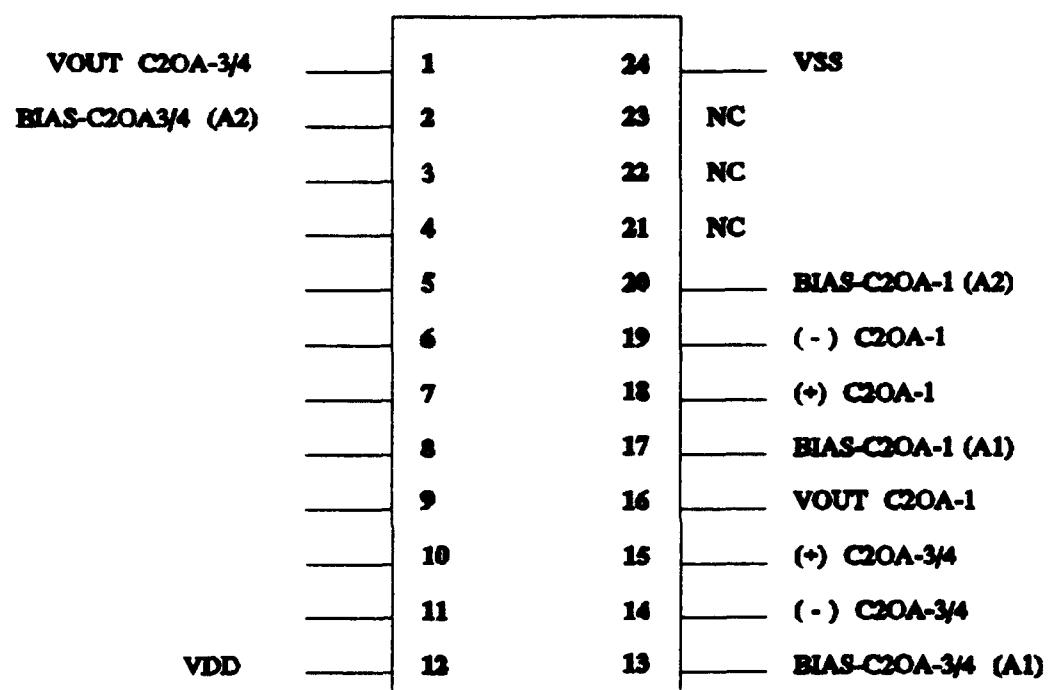
Figure 3.5   Pin Layout of the MLA-6018

The output, inverting input, and non-inverting input terminals for the C2OA-1 are located at pins 16, 19, and 18, respectively. The corresponding terminals for the C2OA-3/4 are located at pins 1, 14, and 15. The A1 and A2 position amplifier biasing terminals are located at pins 17 and 20 for the C2OA-1 and pins 13 and 2 for the C2OA-3/4. Pins 4 through 7 are input terminals for programming α for the C2OA-1, while pins 8 through 11 perform the same function for the C2OA3/4. As described earlier, pin 3 is used to switch between C2OA-3 and C2OA-4. Pins 21 through 24 are not connected.

IV. COMPUTER SIMULATIONS

A. GENERAL

Using circuit data from reference 1, PSPICE simulations were run for the Ferranti Interdesign type P1 op amp and the C20A-1, C20A-3, and C20A-4 configurations as designed on the MLA-6018. Ideal conditons were assumed by selecting ideal components and neglecting the effects of offset voltages. The resultant information was used as a baseline for comparison to experimental results.

B. RESULTS

1. Frequency Response

In Chapter II, it was shown that the 3-dB bandwidth of the C20A-1 should be larger than that for a single op amp. Analysis of the A1 and A2 position amplfiers (Figures 4.1 and 4.2) revealed respective 3-dB bandwidths of 37.6 kHz and 46.3 kHz. This means that when placed in a finite gain voltage inverting configuration with k=50 and applying equation (2.9), the MLA-6018 predicted 3-dB bandwidth should be about 292 kHz. Examination of the simulated response for the C20A-1 (Figure 4.3) yielded a 3-dB bandwidth of about 341 kHz. For the C20A-3 and C20A-4, which each have identical A1 and A2 position amplifiers, equation (2.10) predicts respective 3-dB bandwidths of 940 kHz and 443 kHz. The simulated response for

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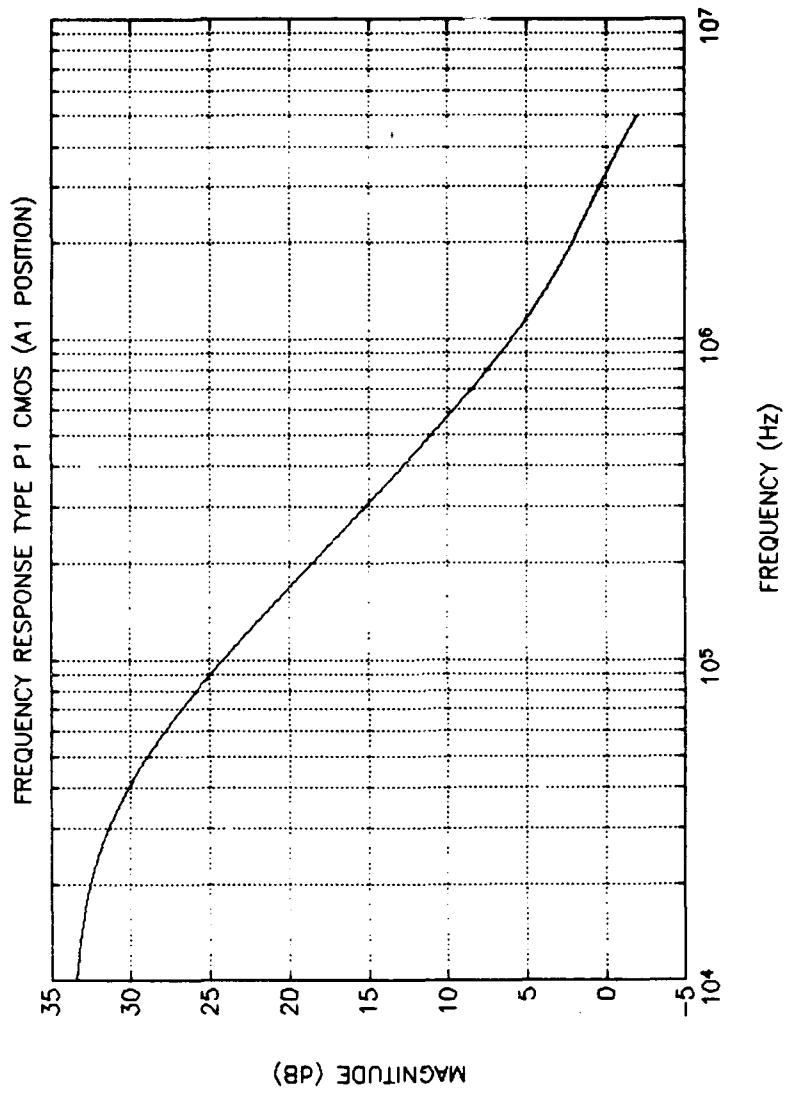
Figure 4.1 PSPICE Frequency Response For Type P1 CMOS Op Amp in the A1 Position on the MLA-6018

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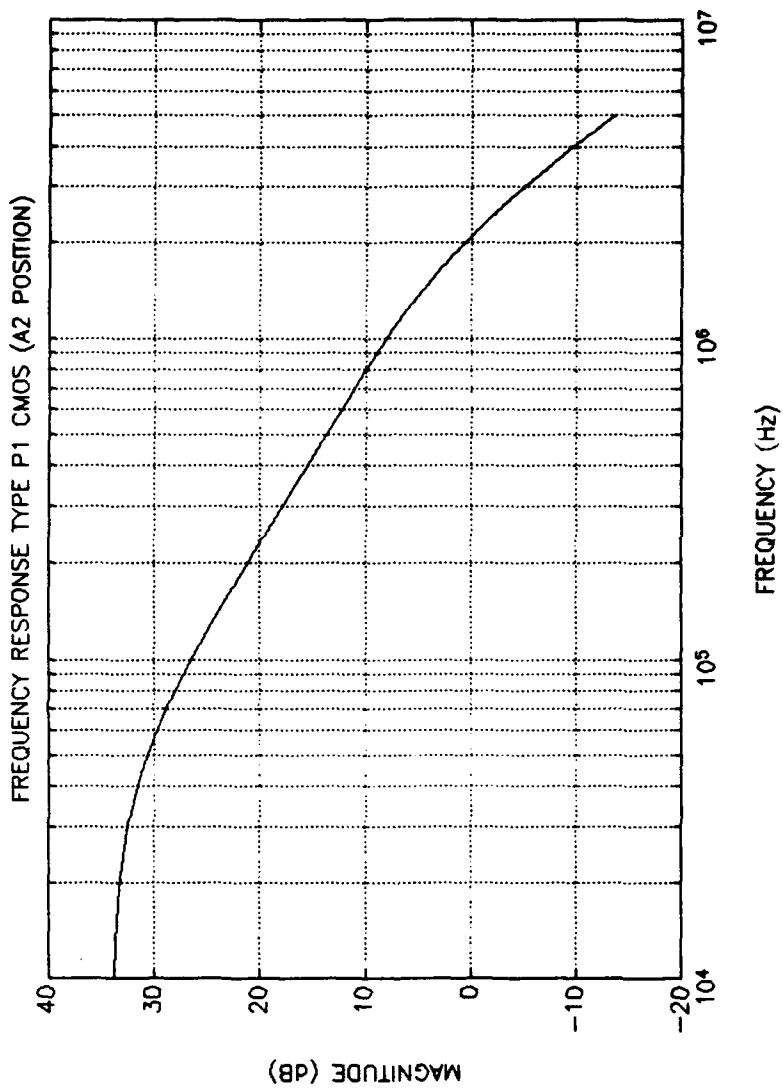
Figure 4.2 PSPICE Frequency Response For Type P1 CMOS Op Amp in the A2 Position on the MLA-6018
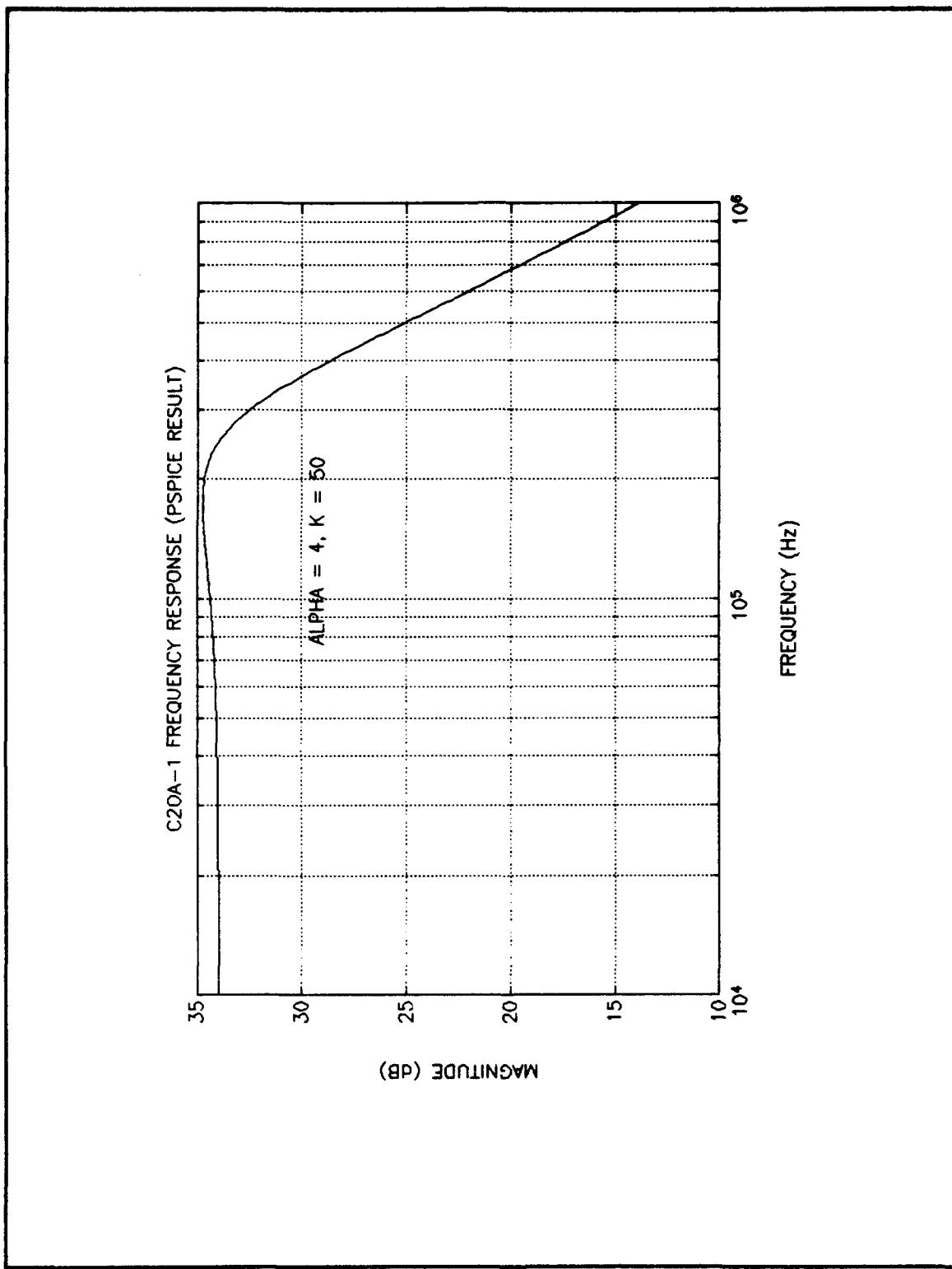
Figure 4.3 PSPICE Frequency Response For MLA-6018 C20A-1

33

the C2OA-3 (Figure 4.4) shows a 3-dB bandwidth of 1.3 MHz, while Figure 4.5, the simulated response for the C2OA-4, shows a 3-dB bandwidth of 1.05 MHz. In all cases, the simulated responses exceed the performance predicted by reference 6. This is probably because the equations used to predict performance are empirically derived, and therefore, have non-ideal op amp performance characteristics incorporated into them.

2. Response to Variations in α

The value of the internal compensation resistance factor α is selected in such a way as to satisfy two basic criteria: 1) stability (Routh-Hurwitz) and 2) a maximally flat frequency response. For the C2OA-1, Routh-Hurwitz is satisfied in the cases where $(1+\alpha) < (1+k)/2$ and a maximally flat response is predicted by the following:

$$Q_p = \frac{(1+\alpha)}{\sqrt{(1+k)}} \qquad (4.1)$$

For maximal flatness, a Q_p of about 0.707 is desired. For a k of 50, both criteria are satisified by $\alpha = 4$.

In the case of C2OA-3, the Routh-Hurwitz requirement is satisfied for instances where $(1+\alpha) > (1+k)^{1/2}$ while maximal flatness is determined from

34
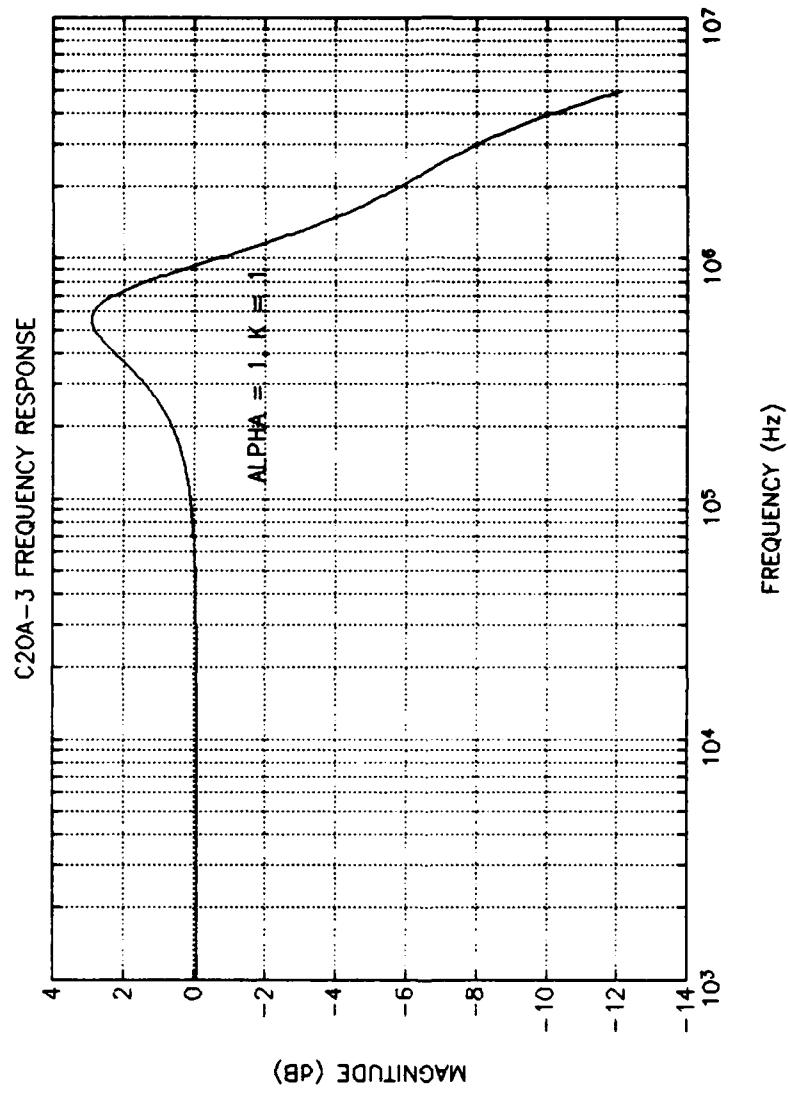
Figure 4.4   PSPICE Frequency Response For MLA-6018 C2OA-3

35
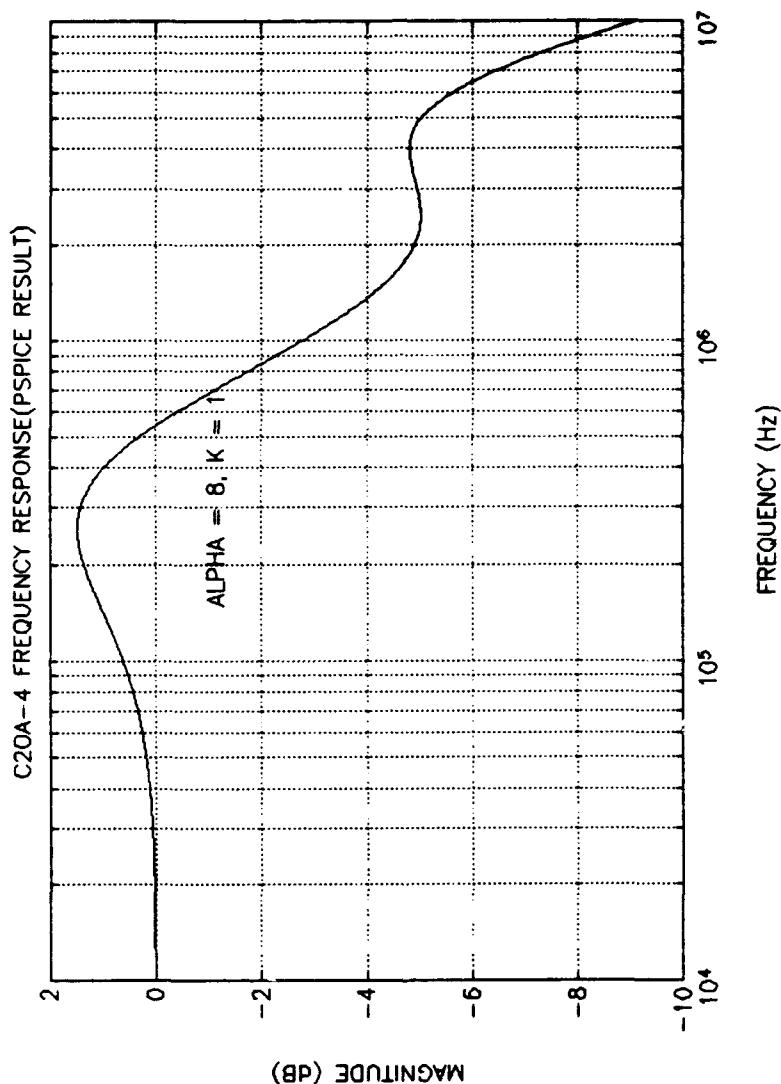
Figure 4.5 PSPICE Frequency Response For MLA-6018 C2OA-4

$$Q_p = \sqrt{(1+k)(1+\alpha)} \qquad (4.2)$$

Assuming a Q_p of 2 and $k = 1$, α must be 1. Values of k greater than 1 result in values of α less than 1 which subsequently result in failing the Routh-Hurwitz criterion.

For the C20A-4, Routh-Hurwitz is satisfied by $(1+\alpha) > 4(1+k)$. Using the Routh-Hurwitz determined value of α as an entering argument, the resultant Q_p can be determined from the following equation:

$$Q_p = \sqrt{\frac{(1+k)}{(1+\alpha)}} \qquad (4.3)$$

The Routh-Hurwitz determined value of α is found from equation (2.5) by assuming $k = 1$. This is necessitated by the limitation on the compensation resistance in the MLA-6018. Any value of k greater than or equal to 2 requires an α greater than or equal to 11, which is beyond the maximum value available on the chip. (Note that a value of $k = 2$ requires an $\alpha = 11$.) Selecting a value of k less than 2 allows the user some flexibility in the selection of α for other C20A-4 applications. Substituting this result into equation (4.3) yields a Q_p of 0.47.

Figures (4.6) through (4.8) demonstrate the effects of the variation of α on the MLA-6018's composites. For C20A-1, increasing α increases both the 3-dB bandwidth and amplitude

of the frequency reponse. Alternately, for the C20A-3 and C20A-4, increasing α decreases both the bandwidth and amplitude of the frequency response.

3. Response to Variation in Bias Current

Bias current in the MLA-6018 is controlled by means of external resistances connected to the biasing terminals of each internal op amp. The change in the amount of current passing through the current mirror is inversely proportional to the change in the value of the attached external biasing resistance. That is to say, if the external resistance value is increased, then the bias current is decreased. Figures 4.9 through 4.11 demonstrate the effects of changing bias resistance.

4. Response to Variations in K

The C20A-1 response to variations in the gain factor k is examined in Figure 4.12. Using equation (2.3), α has been optimized for each case. No analysis of gain variation response was performed for either the C20A-3 or THE C20A-4 due to stability considerations (see Chapter II).

C. SUMMARY

The computer simulations conducted are generally supportive of the composite performance predicted in previous discussions. Better than predicted performance was shown for
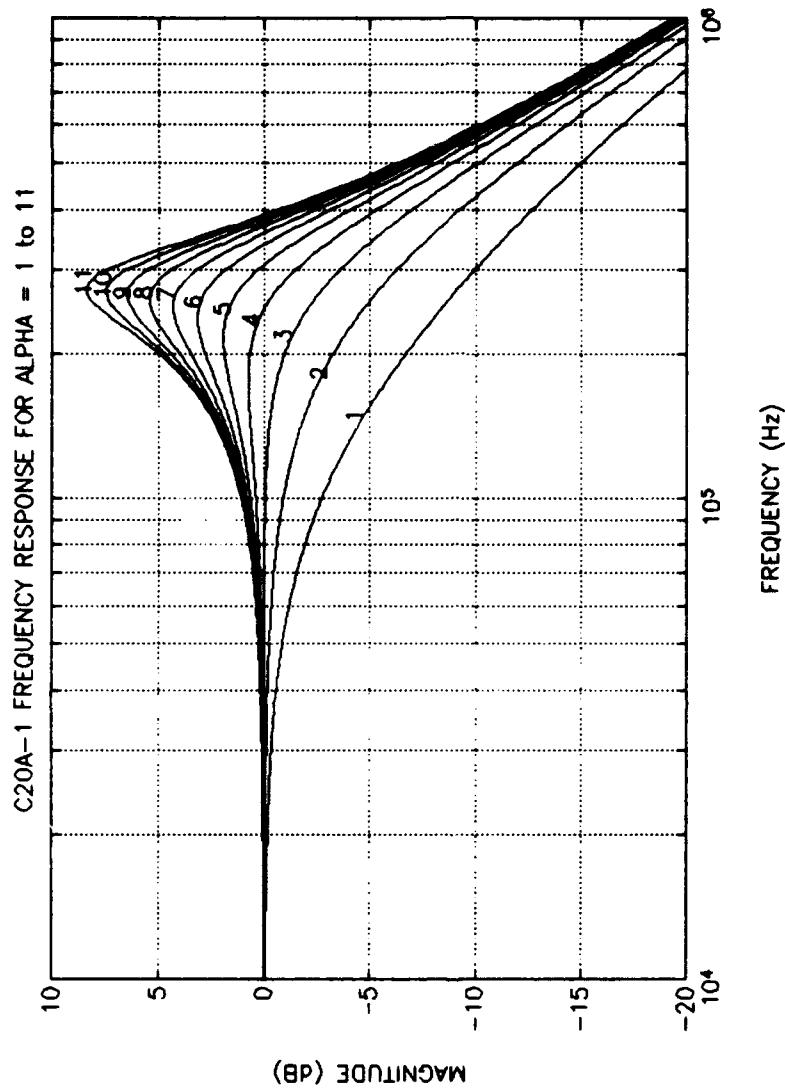
Figure 4.6 PSPICE MLA-6018 C20A-1 Frequency Response Due to Variations in α From One to Eleven

39
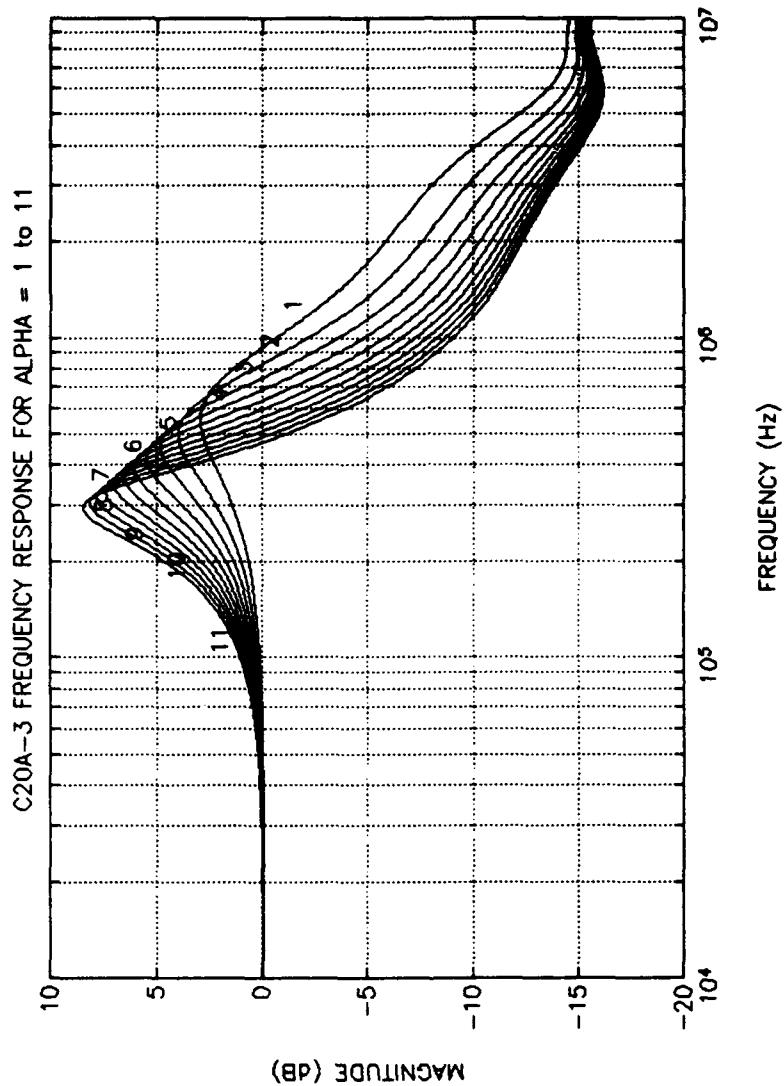
Figure 4.7 PSPICE MLA-6018 C20A-3 Frequency Response Due to Variations in α From One to Eleven

40
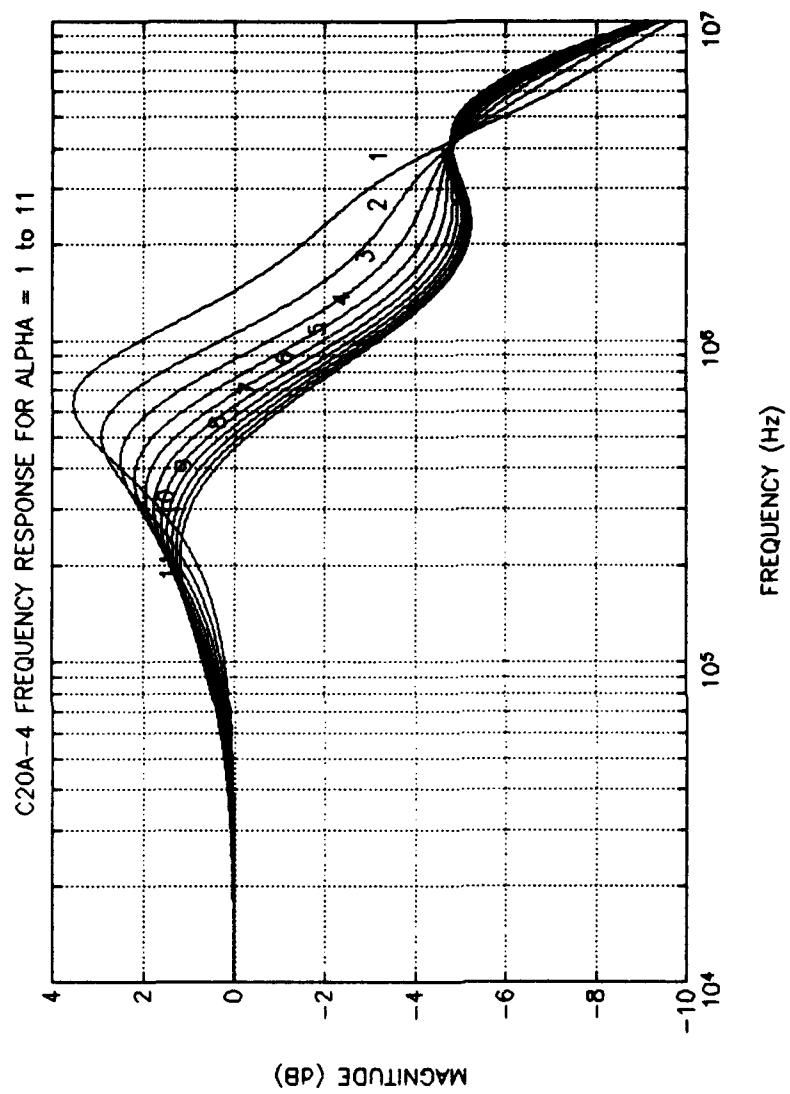
Figure 4.8 PSPICE MLA-6018 C20A-4 Frequency Response Due to Variations in α From One to Eleven

41

C20A-1 FREQUENCY RESPONSE DUE TO VARIATIONS IN RBIAS

Rbias = 25 K OHMS
Rbias = 50 K OHMS
Rbias = 100 K OHMS
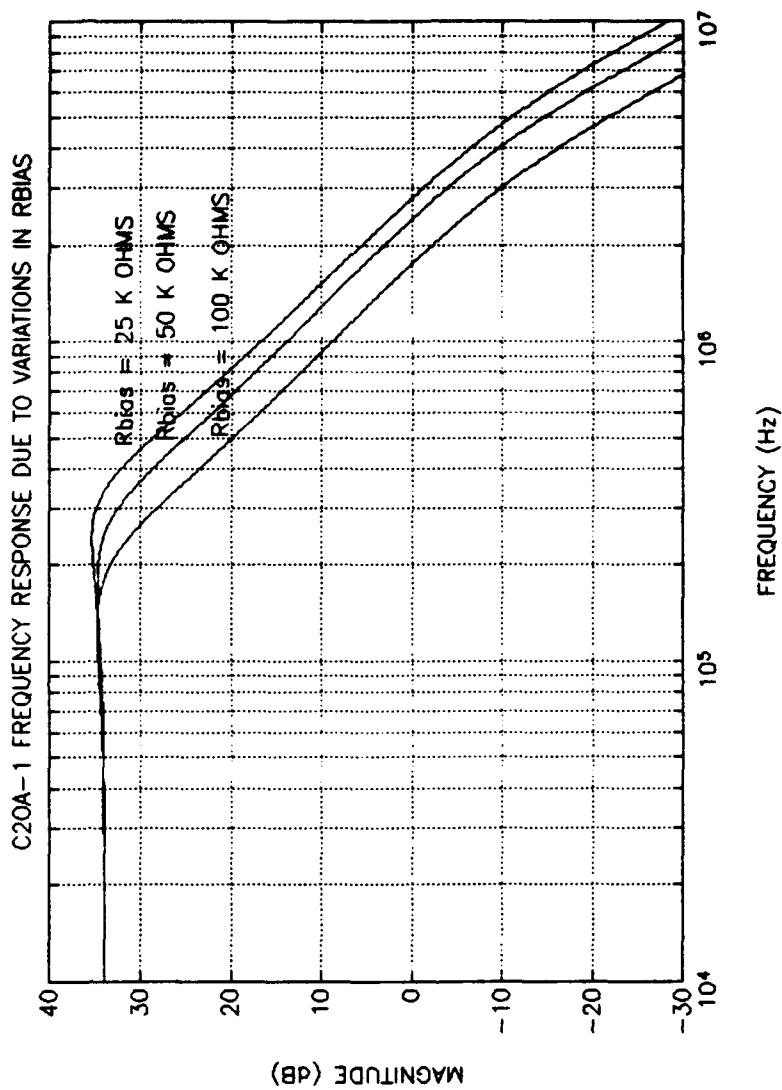
Figure 4.9   PSPICE MLA-6018 C20A-1 Frequency Response Due to Variations in R_{bias}

42
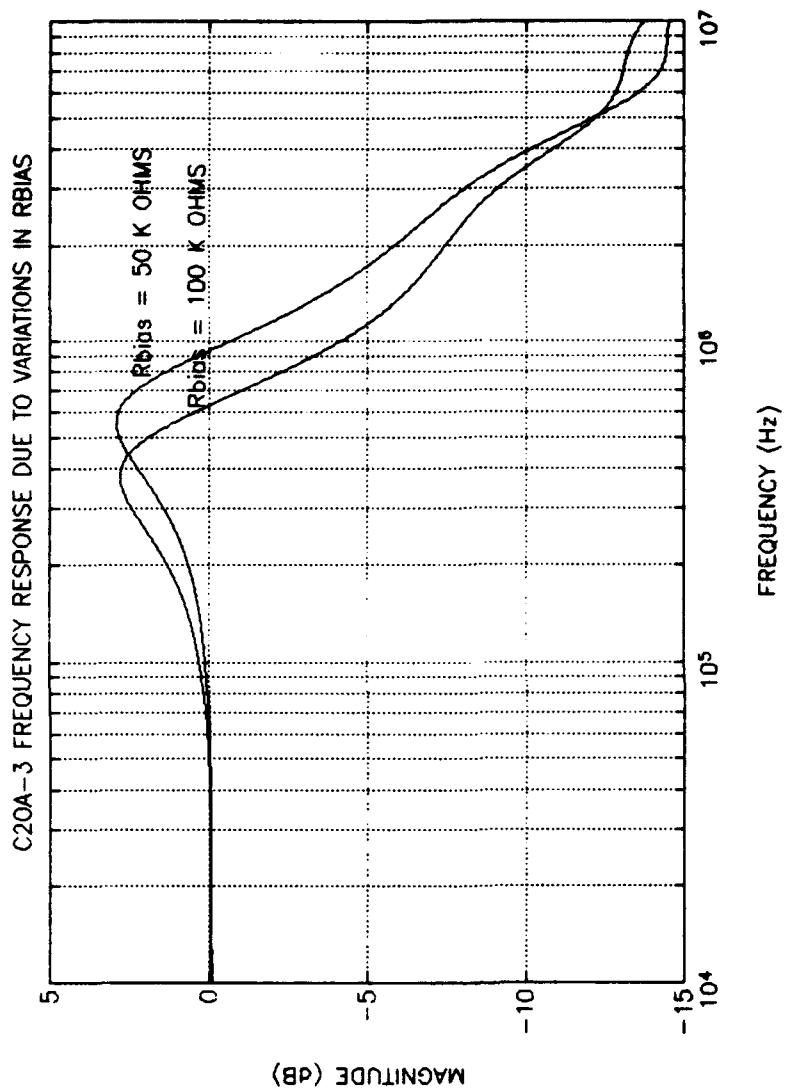
Figure 4.10 PSPICE MLA-6018 C20A-3 Frequency Response Due to Variations in R_bias

43
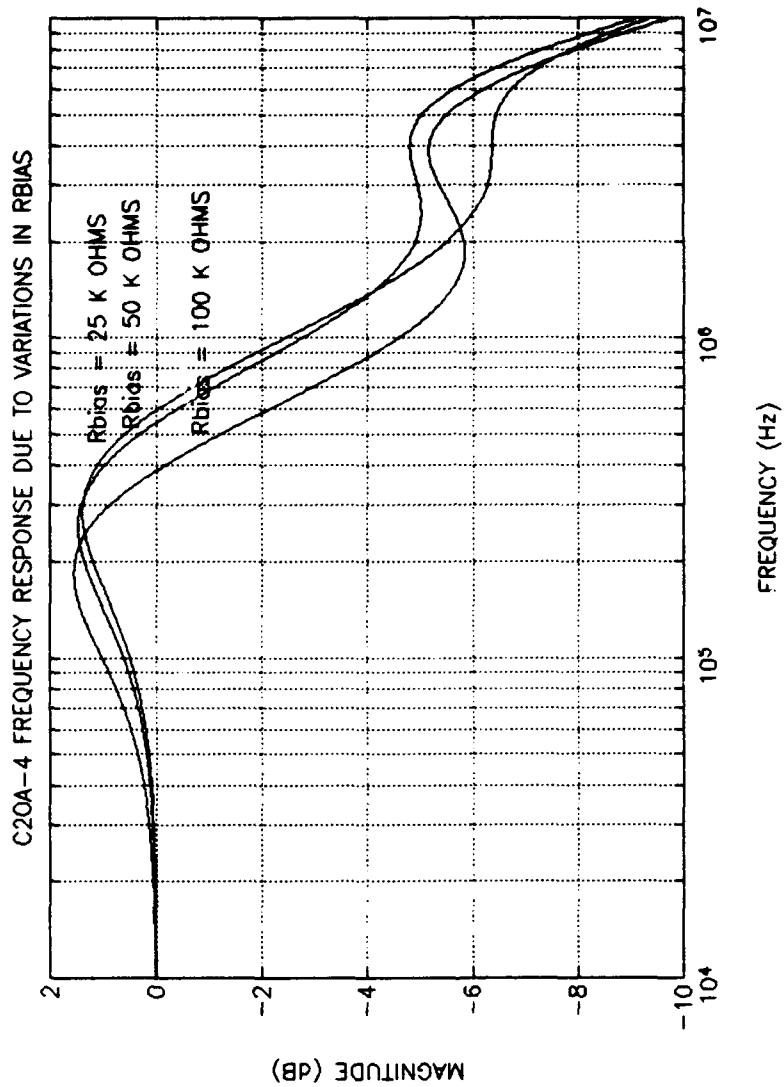
Figure 4.11   PSPICE MLA-6018 C20A-4 Frequency Response Due to Variations in R$_{bias}$
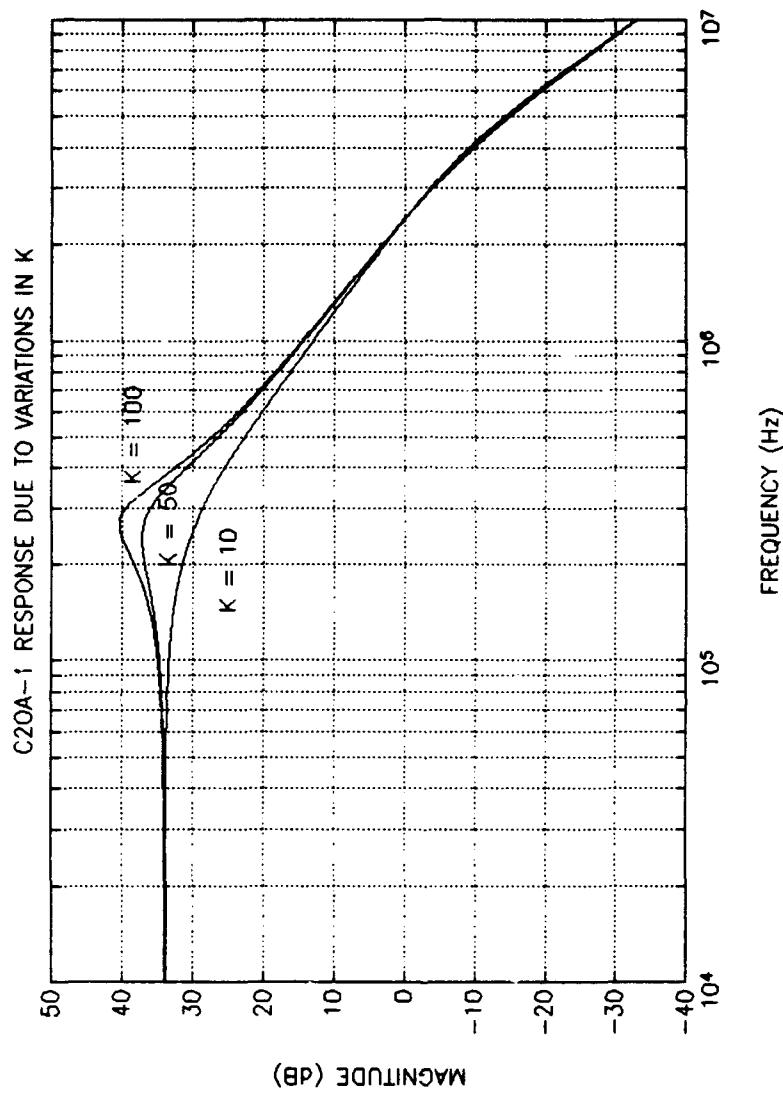
Figure 4.12 PSPICE MLA-6018 C2OA-1 Frequency Response Due to Variations in K

45

frequency response in all cases because the simulations assumed ideal conditions, while the prediction equations were based on experimental observations. There are no equations to predict the performance variations due to variations in α and the bias current, but the simulation results in these areas will provide baseline data for comparison with experimental results.

V. TESTING OF THE MLA - 6018

A.   TEST PROCEDURE

1.   General

MLA - 6018 parameters were measured using the test circuit shown in Figure 5.1. First, the circuit gain, k, and the internal compensation ratio, α, were chosen for each composite in accordance with the stability criteria and maximal flatness concerns discussed in Chapters II and IV. The frequency response using these optimum conditions was then measured and plotted for each composite. Next, using the data from Table 1 (see Chapter III), α was varied from one to eleven and the frequency response was again measured and plotted. Thirdly, the effect of bias current variation on frequency response was examined by varying the value of the external biasing resistances.

Slew rate measurements in response to a square wave input were examined only to verify that the CMOS transistor implementation did in fact yield slew rates higher than those expected from a bi-polar junction transistor implementation.

B.   TEST RESULTS

1.   C20A-1

For a k factor of 50, the optimum value for α, using equation (2.6) and assuming $Q_p = 0.707$, was calculated to be
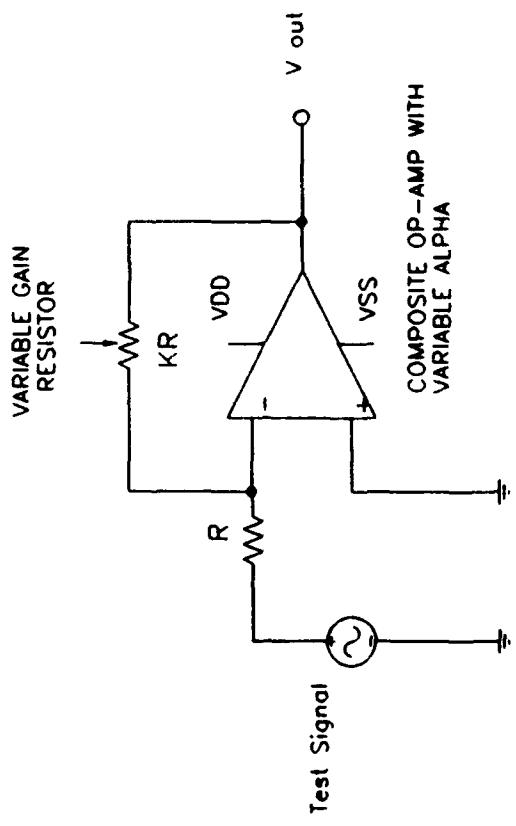
TEST CIRCUIT FOR FREQUENCY RESPONSE
AND SLEW RATE DETERMINATION

Figure 5.1   MLA-6018 Test Circuit

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4.05. Since the MLA-6018 is limited to only integer values of α, the C2OA-1 was tested at $\alpha=4$. From the simulation data in Chapter IV, the 3-dB bandwidth for this configuration was expected to be on the order of 341 kHz. From the experimentally determined frequency response (Figure 5.2), it was found that 3-dB bandwidth for the MLA-6018 C2OA-1 was about 360 kHz. When compared to the simulation circuit response (Figure 5.3) the realized 3-dB bandwidth is larger than the ideal. The realized Q_p is greater than 0.707. The input offset voltage, V_{os}, is one of the likely causes of these differences. When measured for the chip under test, V_{os} was found to be valued at 0.56 millivolts. This means that in the case where the apparent peak value, V_{RMS}, of the output sinusoid is approximately 0.247 volts, the actual portion due to the input is only 0.2469 volts, indicating a 0.2 percent error in the output. This error, however, is not sufficient to explain the observed results. A second source of error may lie in the MLA-6018 programmable resistance network. The design values for resistances R_1 through R10 (see Figure 3.2) may not be accurately implemented on the MLA-6018. Currently, there is no satisfactory method of measuring these resistance values on chip. An additional factor in the response error may also rest with incorrect assumptions regarding the unity gain bandwidths of the type P1 op amps employed in the MLA-6018. Physical representations of the type P1 op amp as configured on the
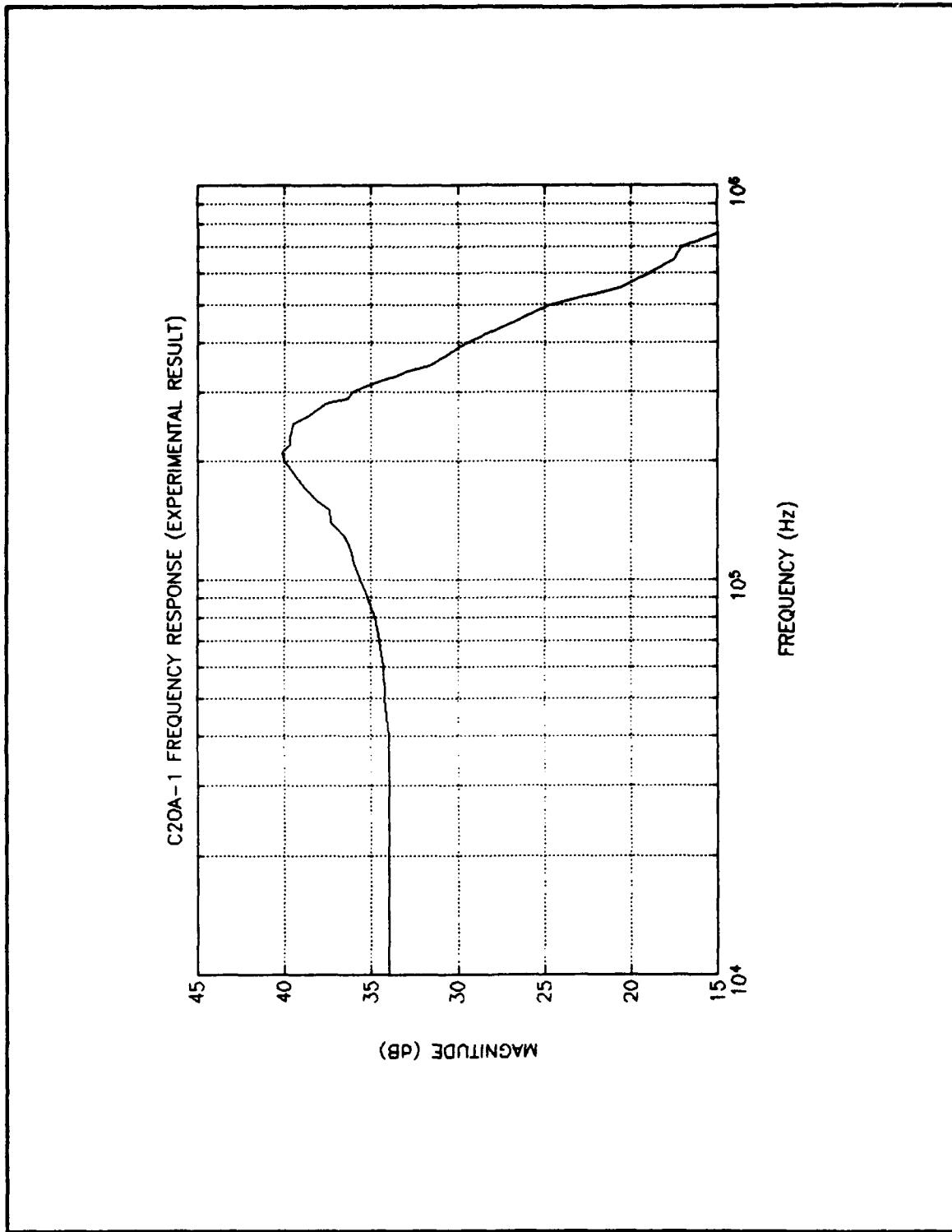
Figure 5.2   C20A-1 Frequency Response, Finite Gain (K=50), Q_p=0.707
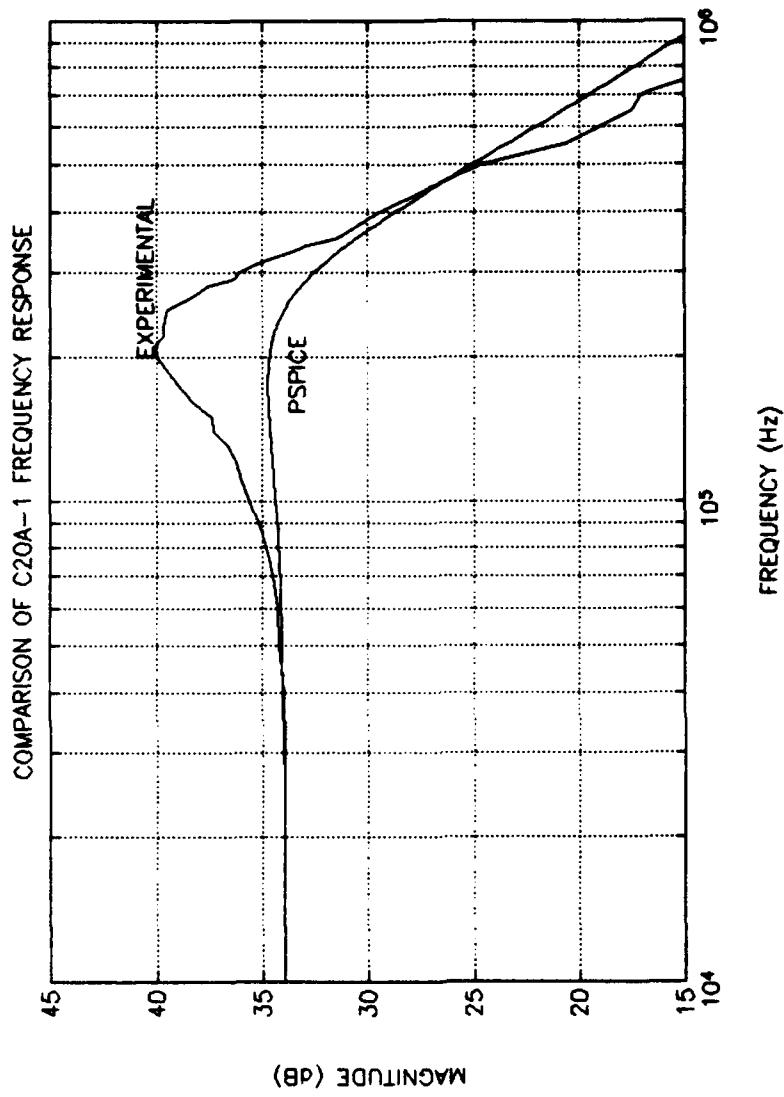
Figure 5.3 PSPICE vs Experimental C20A-1 Frequency Response, Finite Gain (K=50), Q_p=0.707

MLA-6018 are no longer commercially available, thus making it difficult to accurately estimate the performance of the amplifier under laboratory conditions. Using the following equation,

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1+k}} \qquad (5.1)$$

and assuming that ω_1 and ω_2 are equal, ω_p may be used to estimate the unity gain bandwidth for the type P1 op amp. With $\omega_p = 1.13 \times 10^5$ radians, equation (5.1) yields an apparent unity gain bandwidth of 51.4 kHz. While the aforementioned factors probably contribute in aggregate to the overall frequency response error observed, the most significant factor is programmable resistance error.

Based on the simulation results shown in Figure 4.5, it was expected that the MLA-6018 response to variations in α would yield distinct changes. Figure 5.4 shows 3 distinct trends as α increases while k is kept constant. First, there is a gain increase. Second, there is a bandwidth increase. Thirdly, the response becomes "less flat" and moves toward a pronounced peak. Although only three values of α are shown in Figure 5.4, examination of the C20A-1 Routh-Hurwitz stability criteria discussed in Chapter IV reveals that stability is maintained for all values of α, provided k is greater than or equal to 24. It was noted that the MLA-6018's C20A-1, unlike the simulated circuit, becomes unstable for values of α

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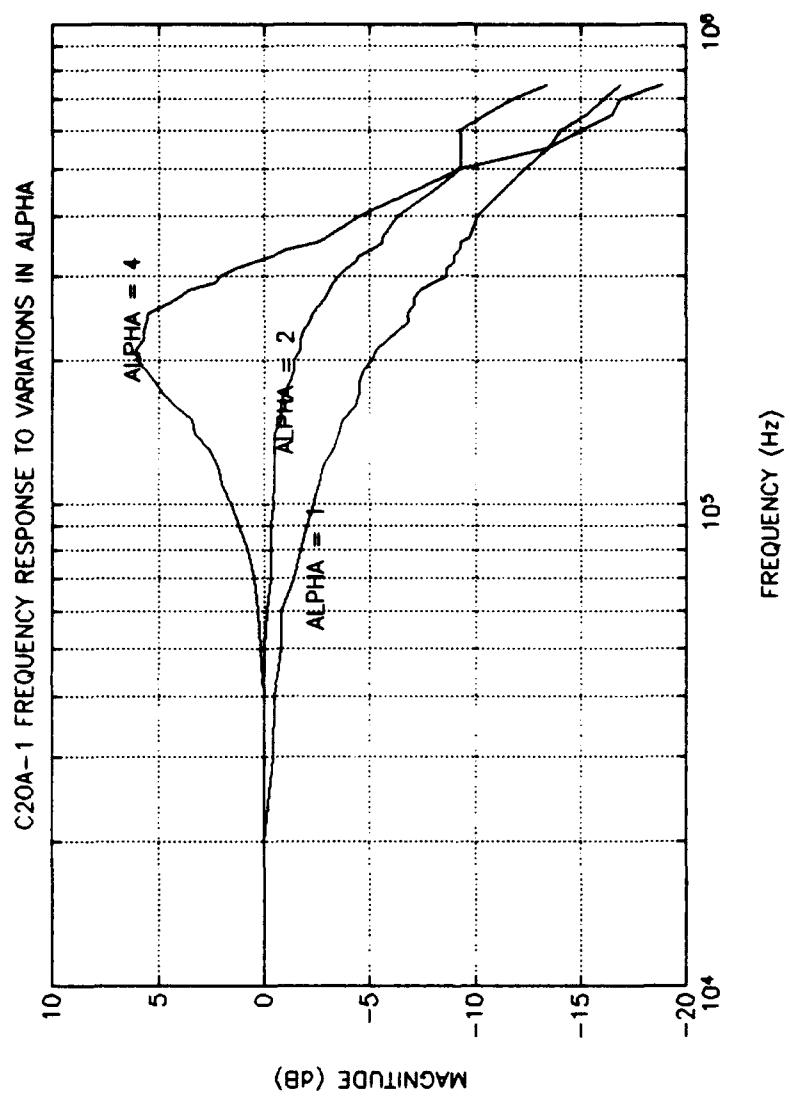
Figure 5.5 C20A-1 Frequency Response Variation as α varies (K is constant)

greater than eight.

Variations in R_{bias} also produce pronounced changes in the C20A-1 frequency response. From Figure 5.5, it should be noted that the bandwidth variation is inversely proportional to the change in R_{bias}; i.e., as R_{bias} increases, bandwidth decreases. The relationship between internal bias current and the external bias resistance is inversely proportional thus, as R_{bias} decreases, bias currents in the current mirrors increase and, as the bias currents increase, the bandwidth also increases.

2. C20A-3

The frequency response for the C20A-3 configuration is shown in Figure 5.6. When compared to the corresponding simulation result (Figure 5.7), differences analogous to those noted in the C20A-1 analysis can be seen. The consistent presence of these differences reinforces the notion of programmable resistance error.

The value of the biasing resistances for the C20A-3 differed significantly from those required for the C20A-1. They also varied from chip to chip. The variance between composite implementations is largely due to stability considerations, whereas the variance from chip to chip is due to manufacturing variations.
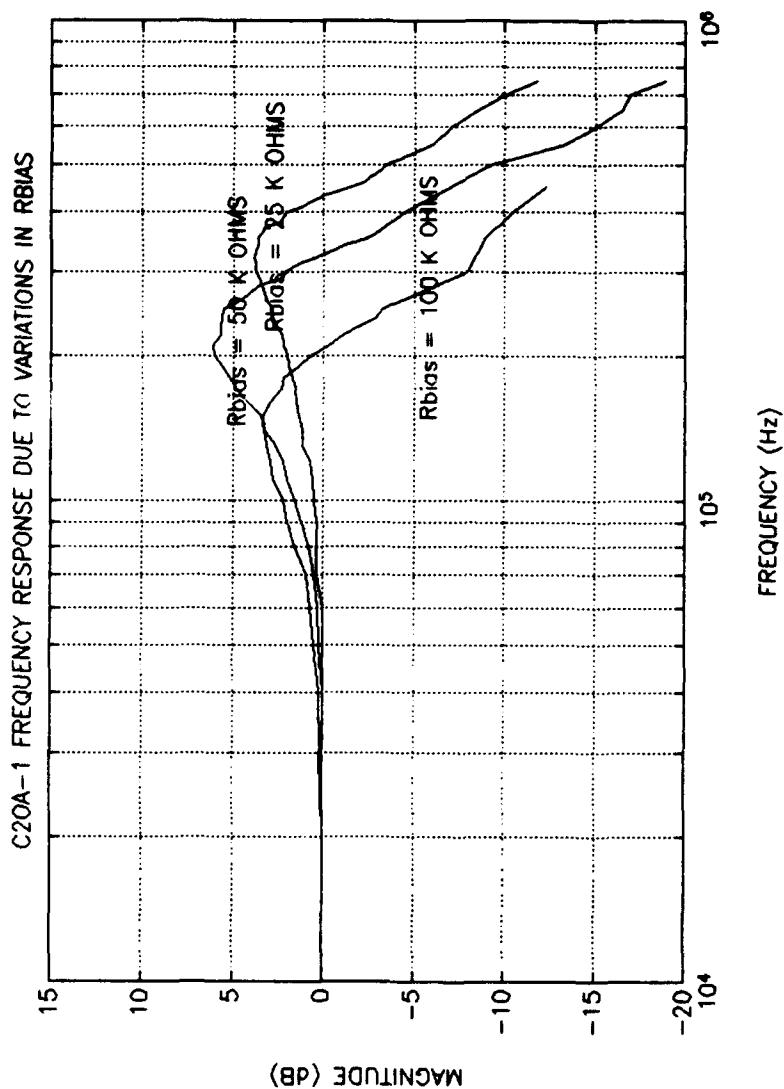
**Figure 5.5   C20A-1 Frequency Response Variation as R_{bias} varies**
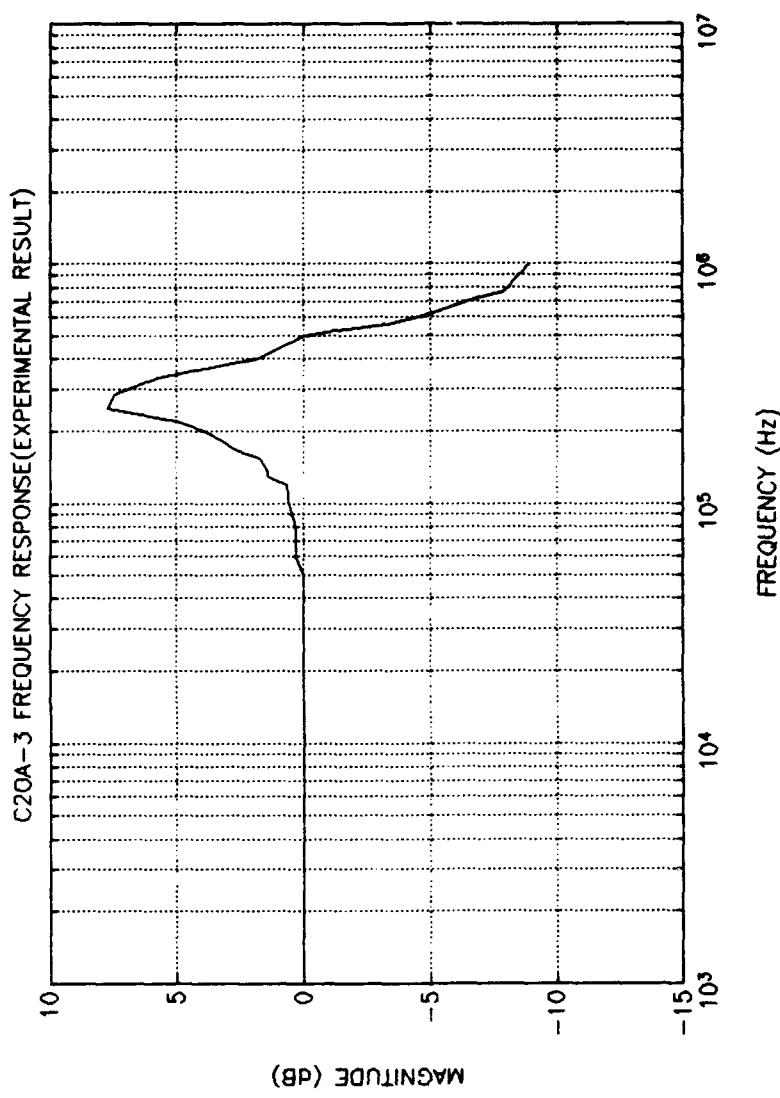
Figure 5.6   C20A-3 Frequency Response, Finite Gain (K=1), $Q_p=2$
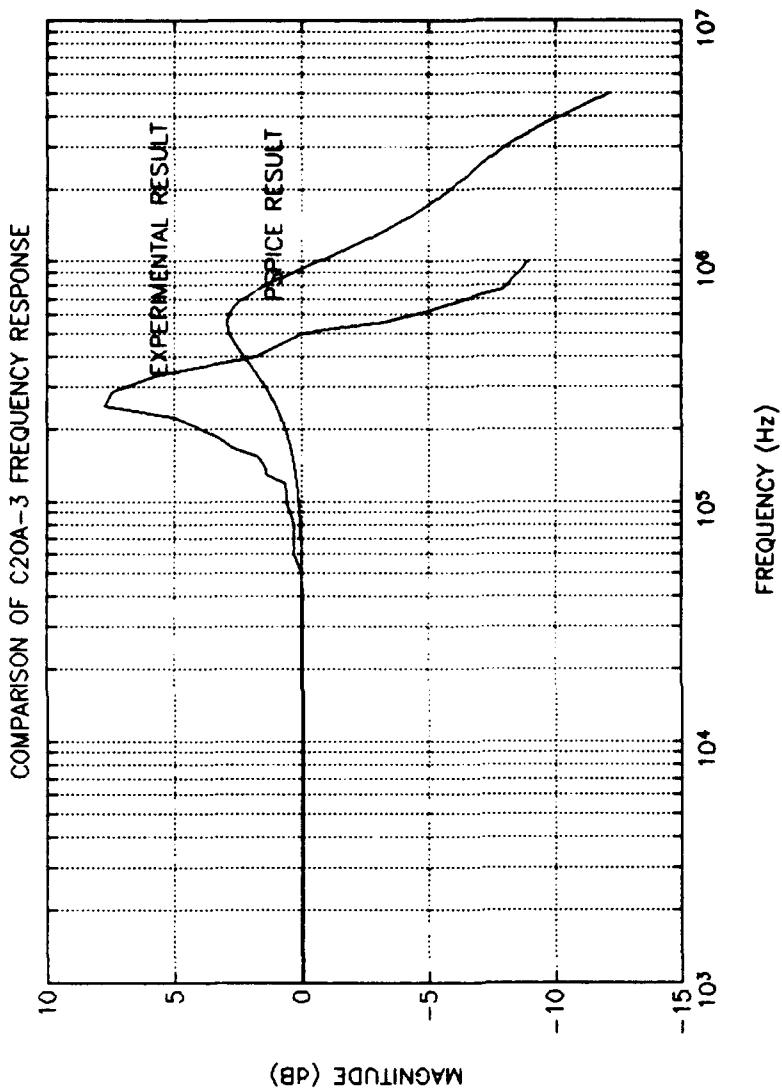
Figure 5.7 PSPICE vs Experimental C20A-3 Frequency Response, Finite Gain (K=1), $Q_p=2$

3. C2OA-4

Although the C2OA-3 and the C2OA-4 share components, the Routh-Hurwitz stability requirement are different for each implentation (see Chapter IV). Hence, the C2OA-4 values for α and k are 8 and 1, respectively. Figure 5.8 shows the experimentally determined frequency response of the MLA-6018 C2OA-4. When compared to the simulation response (Figure 5.9), the 3-dB bandwidth, as in the case of the previously examined amplifiers, is larger than the ideal. The reasoning for this difference follows that of the previously analyzed cases.

C. SUMMARY

Testing began with 30 MLA-6018 chips. One chip exhibited a failed C2OA-1 amplifier, two had failed C2OA-3 amplifiers, and one had a failed C2OA-4 amplifier. This resulted in a net yield of 26 (86.6%) working chips.

Classification of the C2OA-3 and C2OA-4 failures is difficult due to the possibility of the true fault resting in the transmission switching circuitry (see Chapter III).

The MLA-6018 chip generally performs as predicted by theory and previous experiments. The laboratory frequency response results obtained in this study, like the computer simulation results obtained in Chapter IV, exceed those predicted by reference 6.

Composite amplifier gain and bandwidth can be influenced through the use of external biasing resistances. The proper

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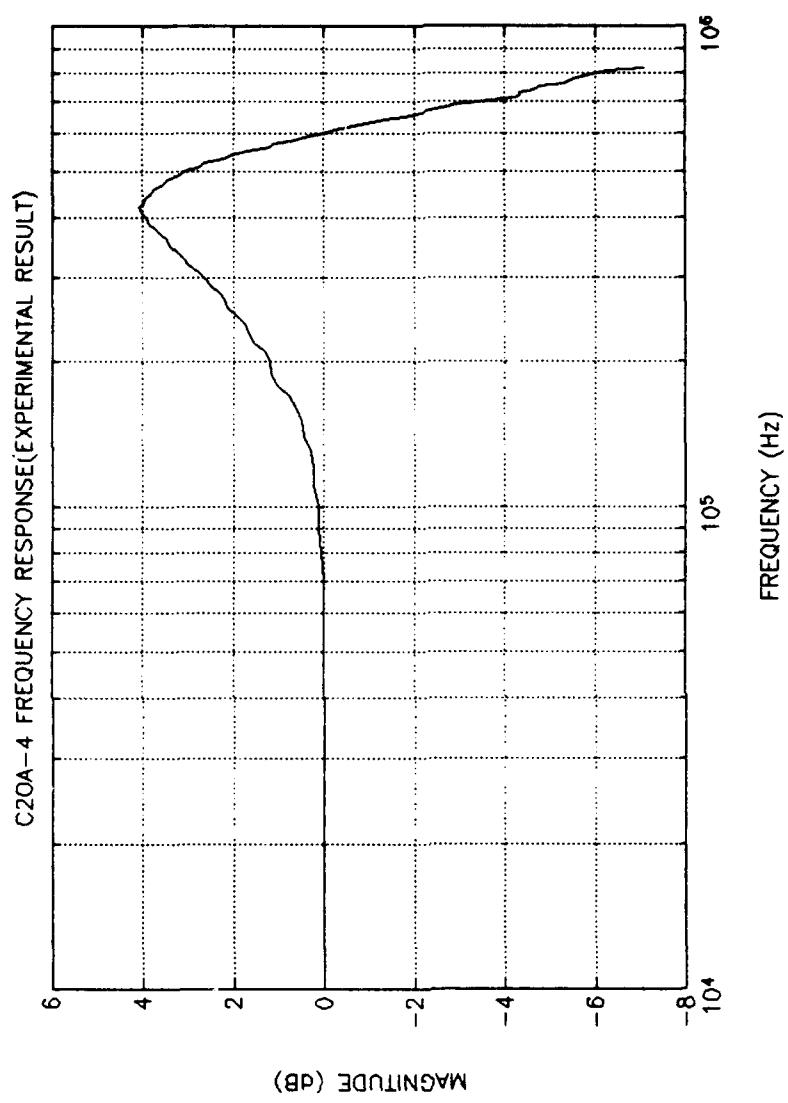
Figure 5.8 C2OA-4 Frequency Response, Finite Gain (K=1), $Q_p=4.24$
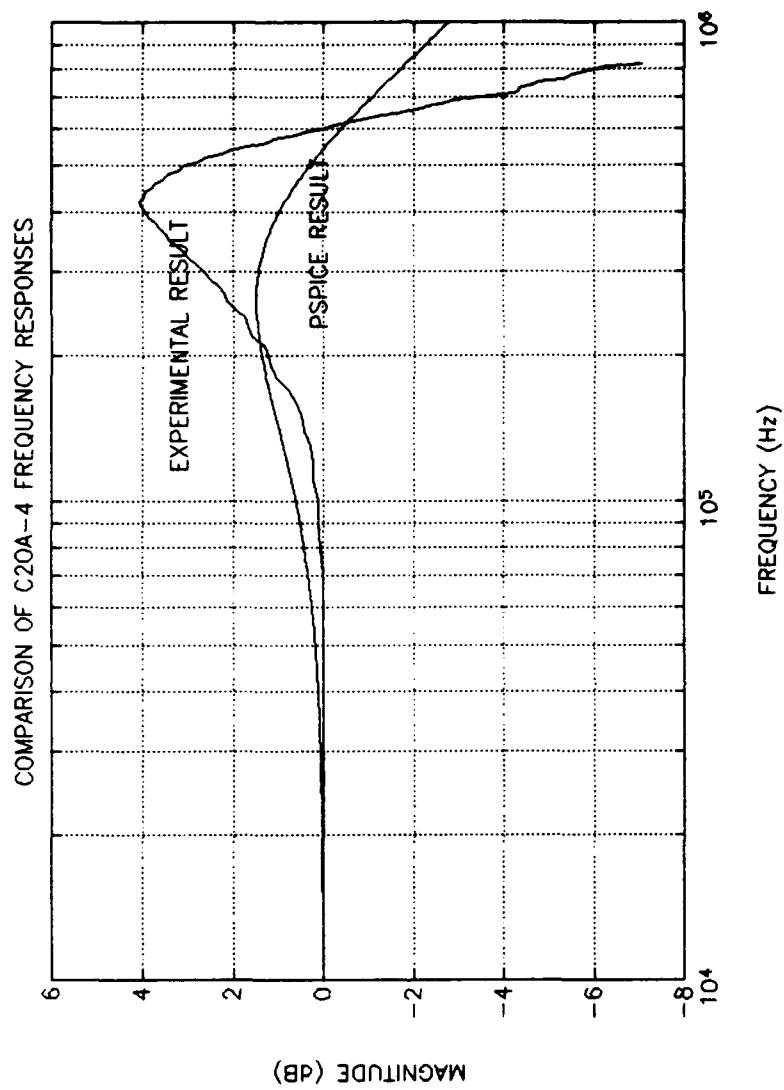
Figure 5.9 PSPICE vs Experimental C20A-4 Frequency Response, Finite Gain (K=1), Q_p=4.24

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values for these external resistances required to achieve a desired result must be derived by trial and error. The presence of the individual biasing terminals for each op amp incorporated into a composite is crucial to the proper performance of the C2OA-3/4 implementations since the input and output stages must be biased separately. The C2OA-1, however, may be biased using a scheme that ties all of the MLA-6018's biasing terminals to one resistor.

The programmable resistance network appears to be a source of problems. Since it is not possible to determine the resistance values implemented via direct measurement, trial and error methods should be used ascertain which program values should used for a desired result, i.e., the Q_p value.

Future improvements to the MLA-6018 concept should include a more reliable resistance network with a greater range of available values. The importance of a greater range of resistance values will be shown in the following chapter.

VI. APPLICATIONS - FILTERS

A. GENERAL

In previous testing, the MLA-6018 was only tested as a finite gain inverter. The goal of this phase of the examination was to evaluate the performance in a specific design condition, namely as an active filter. A filter design was chosen at random and all three composites were examined in the chosen filter configuration first via PSPICE and secondly through experiment. A control implementation using a single LM-741 op amp was built to verify filter performance and provide a baseline for composite op amp performance comparisons.

B. DESIGN AND TESTING

1. Computer Simulations

The filter type chosen for consideration was a multiple feedback bandpass filter with a specified center frequency, f_c, of 37.9 kHz and a Q of 10, as shown in Figure 6.1. Two sets of component value calculation schemes using identical circuit topologies were examined and compared in terms of their success in accurately achieving the design specifications.

In the first scheme, the following equations from reference (5) were applied:
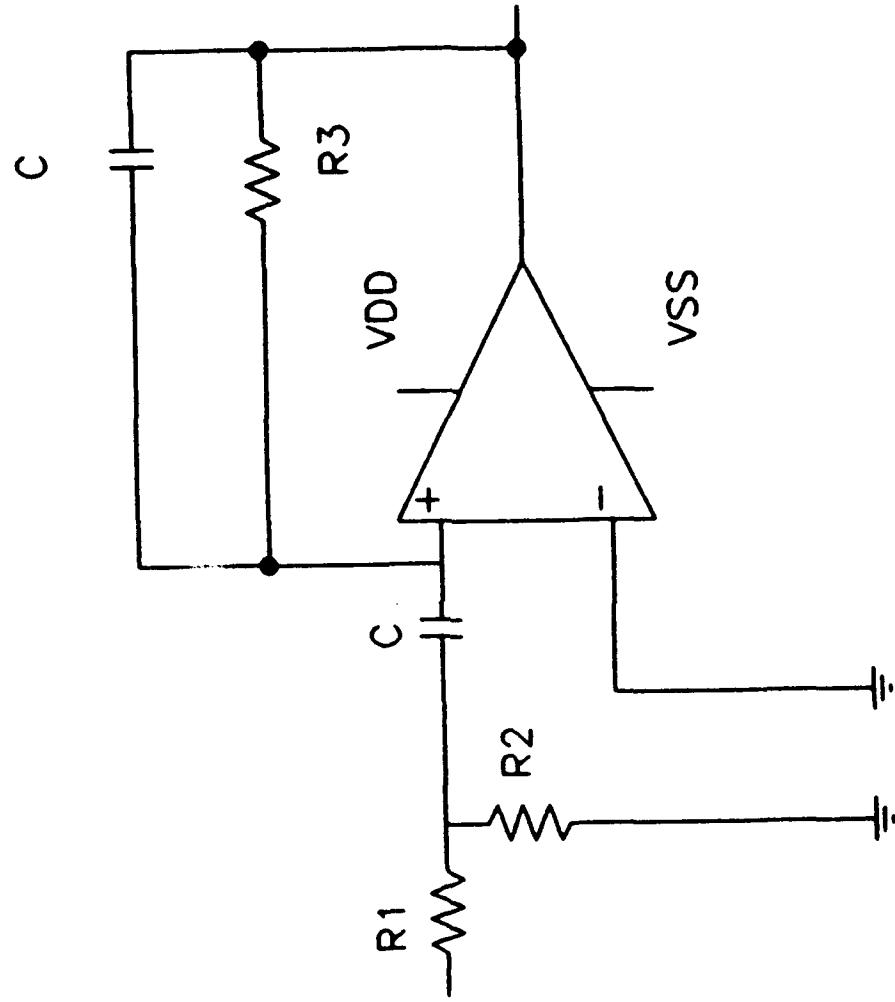
Figure 6.1 Multiple Feedback Bandpass Filter

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$$R_1 = \frac{R_1 + R_2}{R_1 R_2} \qquad\qquad (6.1)$$

where R_i represents the input resistance of the op amp;

$$f_c = \frac{1}{2\pi C \sqrt{R_1 R_3}} \qquad\qquad (6.2)$$

and

$$Q = (1/2)\sqrt{R_3/R_1} \qquad\qquad (6.3)$$

Here, R_i is the entering argument for applying these equations. Typically for a CMOS op amp, R_i is on the order of several hundred kΩ; but for all composites on the MLA-6018, it was assumed to be infinite for ease of calculation. Applying equations (6.1) through (6.3) to the C20A-3, the component values derived are C = 10 pf, R_1 = R_2 = 2.6 kΩ, and R_3 = 1 MΩ. The resultant PSPICE response is shown in Figure 6.2. The apparent error in f_c is insignificant (less than 0.5 percent), while the error in Q is on the order of 3 percent. An alternate calculation scheme from reference (6) that yields a response much closer to the design specifications will be examined in a later discussion.

In order to approach bandpass filter performance, biasing resistance values for the MLA-6018 must be carefully considered. When in the finite gain inverting configuration, the simulated MLA-6018 internal op amps are biased using 50 kΩ resistors. Using similar values of biasing resistance results

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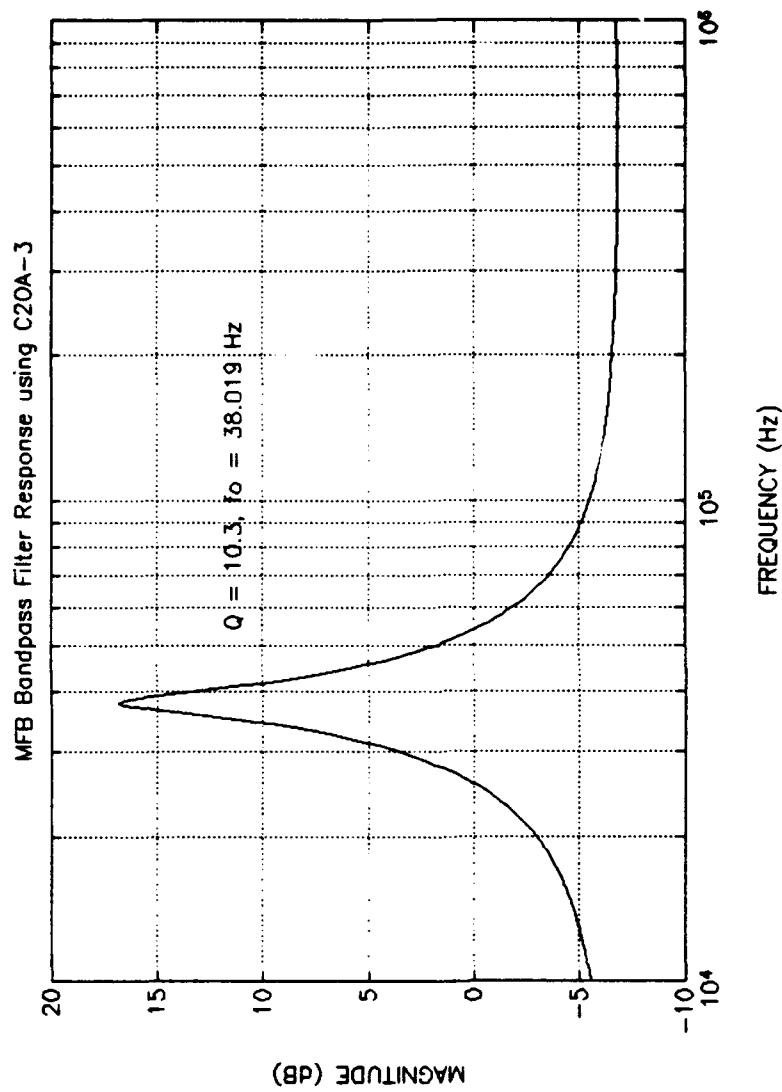
Figure 6.2   PSPICE Multiple Feedback Bandpass Filter Response Using C20A-3 (Scheme Number One)

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in high pass instead of bandpass filter performance. Each internal op amp, therefore, requires separate biasing that must be determined by trial and error. In the case of the C20A-3, the A1 amplifier required a resistance of 175 kΩ and the A2 amplifier used 15 MΩ.

The internal compensation resistance α also plays a significant role in the filter performance. Since the filter was originally designed to be a unity-gain narrowband filter, then, from the Routh-Hurwitz stability criterion for C20A-3 (see Chapter IV), α must be no less than 2. Simply meeting the stability criterion is not, however, a sufficient condition for satisfying bandpass filter performance specifications. Through trial and error, a final α value of 8 was determined to be the optimum for filter performance. Smaller values of α resulted in smaller values of Q as well as shifted center frequencies.

The second scheme involves the following equations:

$$B = \frac{f_c}{Q} \tag{6.4}$$

where B is the filter bandwidth and f_c is the center frequency; alternately, B may be found from

$$B = f_H - f_L \tag{6.5}$$

where f_H and f_L are the filter frequencies above and below the center frequency. The two matched capacitors are found from

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$$B = \frac{1}{2\pi RC} \qquad\qquad (6.6)$$

and the feedback resistor R_2 is found from

$$R_3 = \frac{R_1}{2Q^2 - 1} \qquad\qquad (6.7)$$

The value of R_1, which is arbitrarily chosen, is half the value of R_3.

From equations (6.4) through (6.7), the filter capacitances were set at 0.35 nF, R_2 at 503 Ω, R_1 arbitrarily set at 100 kΩ, and R_3 set at 200 kΩ. The resultant PSPICE response is shown as Figure 6.3. As in the case of the first calculation scheme, both the internal op amp biasing and internal compensation resistance values significantly affect filter performance. Also, as in the previous scheme, both quantities had to be derived by trial and error. The A1 amplifier was biased with a 1.8 MΩ resistance and the A2 amplifier was biased with a 5 MΩ resistance. The optimum value of α was determined to be 5. This result yields an error in f_c of less than 0.5 percent and virtually no error in Q. The same scheme using C = 1.2 nF, R_1 = 35 kΩ, R_2 = 50 Ω, and R_3 = 70 kΩ was evaluated using a single LM-741 op amp (Figure 6.4).

2. **Experimentation**

Based on the PSPICE simulation results, the second calculation scheme was used for constructing a laboratory

MFB BANDPASS FILTER RESPONSE FOR C20A-3

Q = 10, fo = 38.019 KHz

FREQUENCY (Hz)

MAGNITUDE (dB)
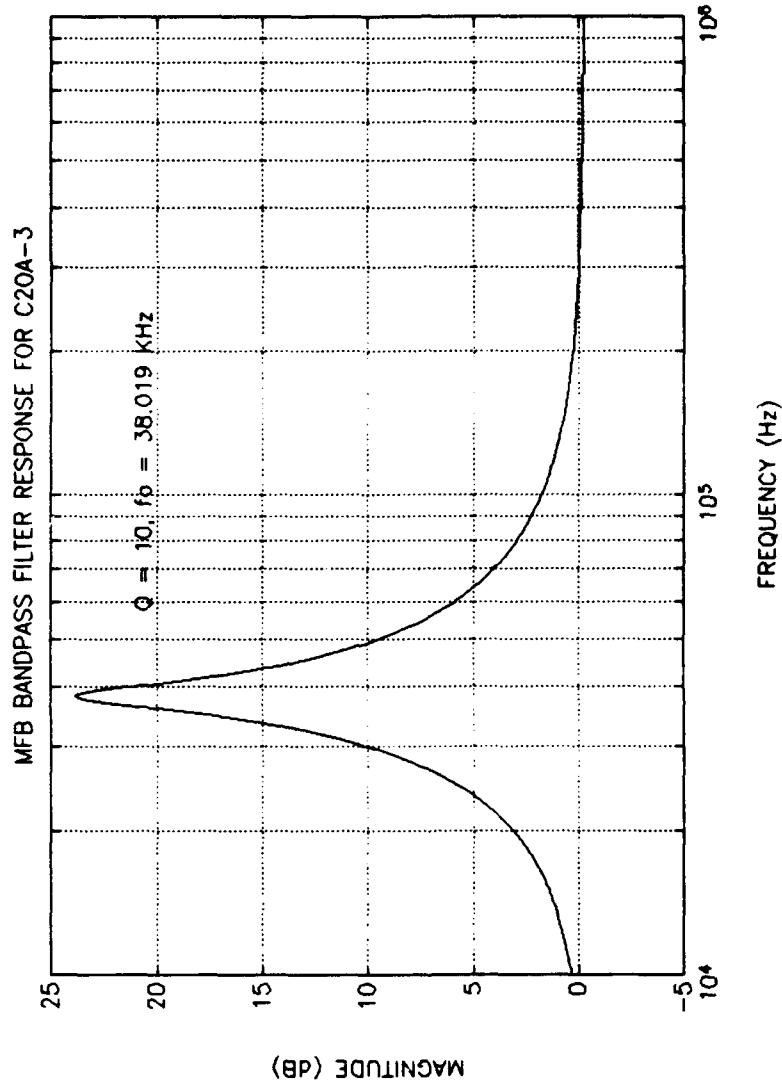
Figure 6.3 PSPICE Multiple Feedback Bandpass Filter Response Using C20A-3 (Scheme Number Two)
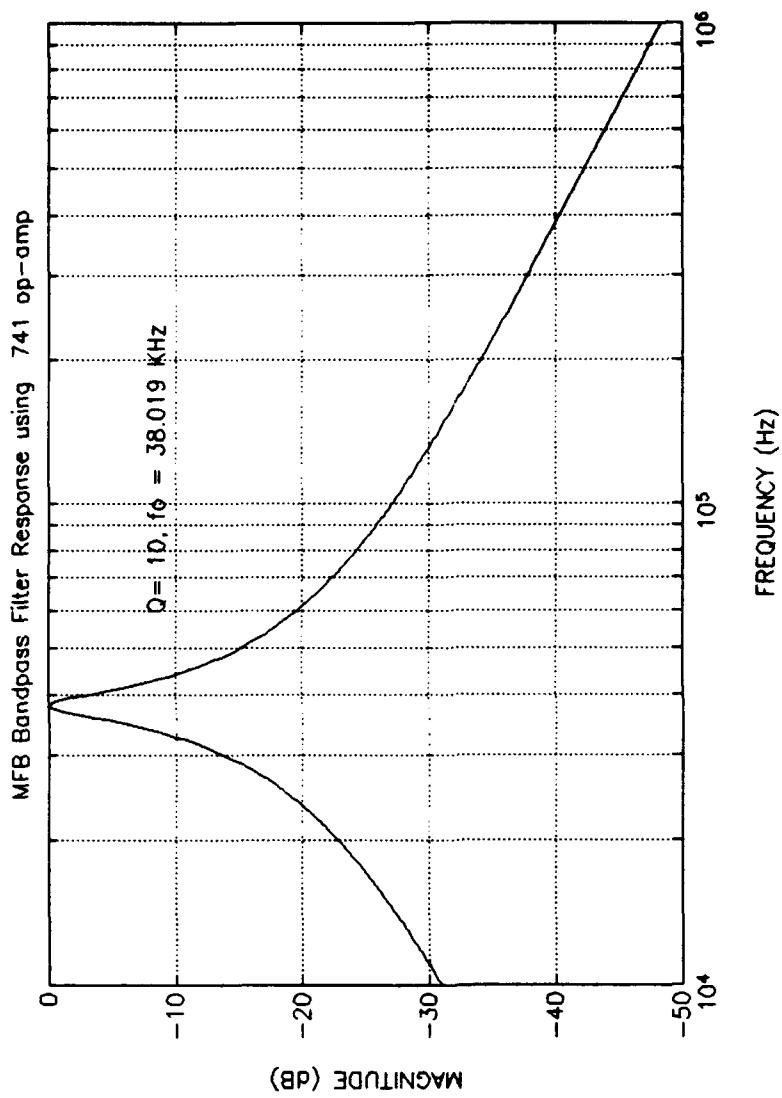
Figure 6.4 PSPICE Multiple Feedback Bandpass Filter Response Using LM-741 Op Amp

model of the filter for test and evaluation. Figure 6.5 is the experimental result obtained using a single LM-741 op amp compared to the response shown in Figure 6.4. While the center frequency is very nearly 37.9 kHz, Q at approximately 19.3 is nearly twice the specified design value. This is not an altogether unexpected result since the composite was expected to yield an improved overall performance.

From the techniques used to obtain Figures 6.2 and 6.3, several attempts were made to construct the bandpass filter using all composite implementations on the MLA-6018. In all cases the response obtained indicated high pass instead of bandpass filter performance. Despite varying the bias resistances from a few hundred ohms to values well in excess of 10 MΩ, filter performance was unsatisfactory. The value of α was subsequently varied from zero to eleven with a slight improvement in the performance at $\alpha = 11$. While it is belived that bandpass performance can be obtained for values of α beyond 11, experimental results indicate the MLA-6018 is a poor candidate for unity-gain narrow-band filter applications.

C. SUMMARY

Theoretically, the MLA-6018 is capable of fulfilling a role as a multiple feedback bandpass filter. Experimentally, it cannot satisfactorily perform as a filter. The reasons for this failure are the same as those regarding finite gain performance as discussed in Chapter V. In addition to
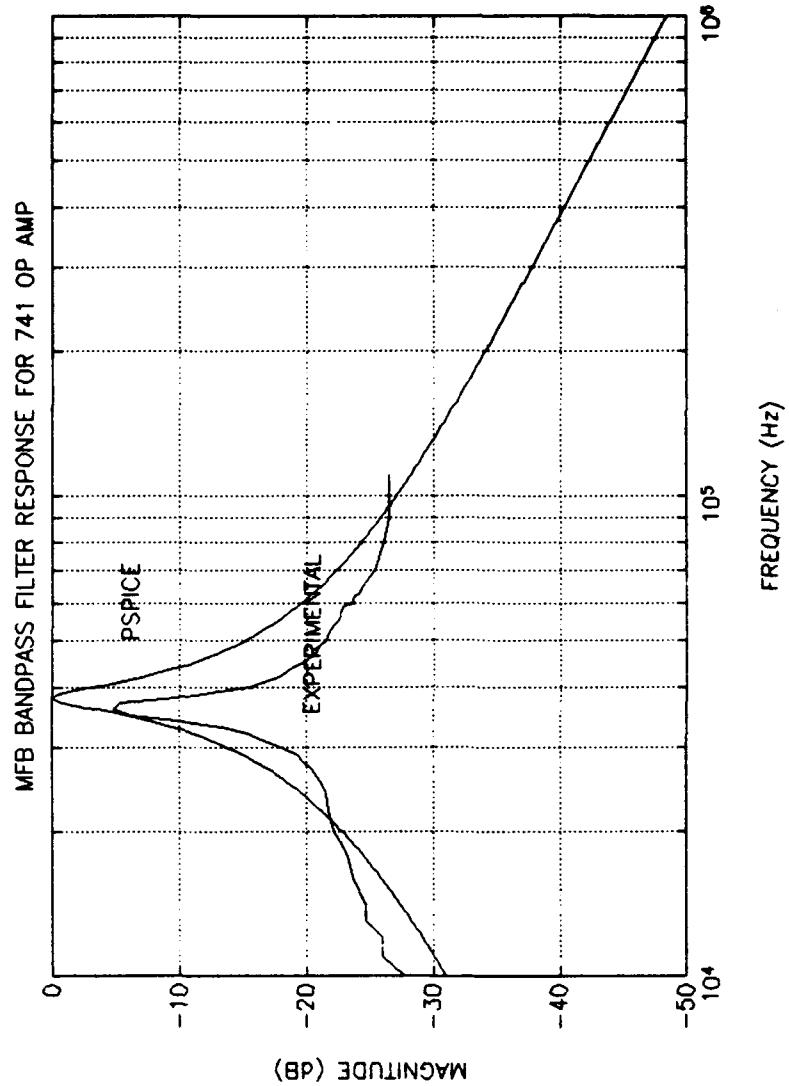
Figure 6.5 PSPICE vs Experimental Multiple Feedback Bandpass Filter Response Using LM-741 Op Amp

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inaccurate internal compensation resistance values, the limited range of resistance values should also be considered as contributing to the MLA-6018's poor performance. As α is increased, the Q can be increased. Without a greater range of α values, it is difficult to estimate when the MLA-6018 could achieve satisfactory filtering performance. Similarly, as the bias resistance value is adjusted, Q is affected. This effect, however, is not as great as that of α.

VII. CONCLUSIONS

The objectives of this study were to determine if composite op amp topologies could be satisfacorily implemented on a chip and, if so, evaluate the performance of the composites.

After a basic subject introduction in Chapter I, Chapter II discussed the basic differences between single and composite op amps, concluding that the composite could be expected to offer improved performance over the single. Although the composite was expected to offer improved performance over the single op amp, it was also noted that the general non-ideal performance characteristics of the two were not appreciably different. This was particularly true in terms o' the need for proper frequency compensation.

Chapter III presented the design and construction of the composites on the MLA-6018 chip. A brief description of the fabrication process was offered without evaluation. Recommendations regarding chip fabrication, however, will be offered later in this chapter.

Chapter IV covered the computer simulations of the MLA-6018. PSPICE was used to obtain plot data. This provided baseline data that was used to evaluate the experimental results obtained in Chapter V. The basic PSPICE code for the

C2OA-1, C2OA-3, and C2OA-4 are provided as an appendix to this study.

Experimentation were described Chapter V. As discussed earlier, the data obtained in this chapter was compared to the corresponding simulation data from Chapter IV. In general, the MLA-6018 did offer improved performance in terms of increased useful bandwidth. The Q, however, was higher than expected in all cases. After considerable thought and examination, I concluded that the principal cause for this discrepancy rested with inaccuracies in the implemented internal compensation resistances. The pin layout of the MLA-6018 does not support the examination of individual components, thus I could not measure the true values of the internal resistances. The resolution to these problems will be later addressed as a recommendation.

A multiple feedback bandpass filter (MFB BPF) application was examined in Chapter VI. PSPICE simulations for the C2OA-3 and single LM-741 op amps provided baseline data for comparison to experimental results. Prior to testing the MLA-6018, an MFB BPF using a single LM-741 op amp was constructed and tested to provide additional baseline data. Testing of the MLA-6018 C2OA-3 in the MFB BPF configuration yielded less than satisfactory results. The C2OA-3 consistently exhibited high pass instead of bandpass filter performance despite adjustments to biasing and internal compensation resistances. The most probable cause for these results is two-fold. First,

as discussed earlier, there are inaccuracies within the internal compensation resistance network. Secondly, even if the internal compensation resistances were accurate, the MLA-6018 may require much higher values of resistance in order to achieve bandpass performance.

From the aforementioned dicussions, the following recommendations are offered to improve study and performance of the MLA-6018 and its successors (if any). The fabrication process for this chip is very useful in terms of simplicity, because it allows simple interconnection of components. Although it does not allow for extremely complex circuit implementation, it is more than adequate for study applications and should continue to be used for such purposes. Study of this type chip could be enhanced, however, by allowing additional pins to be used for examination of individual on-chip components such as resistors. The experience gained from this study suggests that there are resistance value problems that must yet be ironed out. The options available for accomplishing this include using laser trimmed resistances or using parisitic-free switched capacitances. The use of laser trimmed resistances will achieve accurate values but also incur a much higher cost of fabrication for which the return is not commensurate. Switched capacitors offer promise and are available through the semi-custom design process for a fraction of the monetary and chip space costs for the laser trimmed resistances.

In conclusion, this study has verified the theory of composite amplifiers and has proven that composites can be successfully integrated on a single chip. The MLA-6018 is not perfect, but it works.

APPENDIX

This appendix contains the PSPICE code for the three composite circuit topologies used on the MLA-6018.

```
* C20A-1
* Based on Ferranti Interdesign type P1 OP-AMP
*
.OPTIONS ITL4=40
.OPTIONS RELTOL=.01
* TRANSISTOR MODELS
***********************************
**NMOS
.MODEL MEDN NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415
+UTRA=0.25 RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10
+VMAX=4.8E4 NEFF=4.0 XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=8.7N
***************************************************
.MODEL LGN NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415
+UTRA=0.25 RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10
+VMAX=4.8E4 NEFF=4.0 XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=7.6N
*******************************************
*******************************************
**PMOS
.MODEL MEDP PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF-
=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=8.7N
*********************************************
.MODEL LGP PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF=1-
0.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=7.5N
*
*
* Circuit Description (A1 POSITION OP-AMP)
*********************************************
M0311    2    7    6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0312    2    7    6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0321    9    8    6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0322    9    8    6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
```

```
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0351     6    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12

M0352     6    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0361     5    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0362     5    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0331     3    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0341    10    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0342    10    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0343    10    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0371     2    2    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0381     9    2    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
M0391     3    2    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
M0401    10    9    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
M0402    10    9    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=18CU PS=163U NRD=0.12 NRS=0.25
M0403    10    9    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
*
*
*(A2 POSITION OP-AMP)
*****************************************
M0411    12    10    11    21    LGP L=24.0U W=290.0U AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0412    12    10    11    21    LGP L=24.0U W=290.0U AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0421    14     0    11    21    LGP L=24.0U W=290.0U AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0422    14     0    11    21    LGP L=24.0U W=290.0U AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0451    11    15     4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0452    11    15     4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
```

```
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0461      15      15      4     21     MEDP  L=12.0U  W=60.0U  AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12

M0462      15      15      4     21     MEDP  L=12.0U  W=60.0U  AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0431      16      16      4     21     LGP   L=24.0U  W=290.0U  AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0441      17      16      4     21     LGP   L=24.0U  W=290.0U  AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0442      17      16      4     21     LGP   L=24.0U  W=290.0U  AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0443      17      16      4     21     LGP   L=24.0U  W=290.0U  AD=8700P
AS=6235P
+PD=640U PS=623U NRD=0.1 NRS=0.1
M0471      12      12      1     22     LGN   L=24.0U  W=155.0U  AD=4650P
AS=3335P
+PD=370U PS=353U NRD=0.08 NRS=0.08
M0481      14      12      1     22     LGN   L=24.0U  W=155.0U  AD=4650P
AS=3335P
+PD=370U PS=353U NRL=0.08 NRS=0.08
M0491 16   12      1  22  LGN L=24.0U W=155.0U AD=4650P AS=3335P
+PD=370U PS=353U NRD=0.08 NRS=0.08
M0501      17      14      1     22     LGN   L=24.0U  W=155.0U  AD=4650P
AS=3335P
+PD=370U PS=353U NRD=0.08 NRS=0.08
M0502      17      14      1     22     LGN   L=24.0U  W=155.0U  AD=4650P
AS=3335P
+PD=370U PS=353U NRD=0.08 NRS=0.08
M0503      17      14      1     22     LGN   L=24.0U  W=155.0U  AD=4650P
AS=3335P
+PD=370U PS=353U NRD=0.08 NRS=0.08
*
.PARAM ALPHA = 4
*.STEP PARAM ALPHA 1,11,1 (THIS COMMAND IF EXECUTED, WILL
DEVELOP
* FREQUENCY RESPONSES FOR ALPHA FROM 1 TO 11)
*
* RESISTORS (R2 variable)
R1           7       0              12.5K
R2           7      10              {ALPHA*12.5K}
R3           8      19              10K
RBIAS1       5       0              50K
RBIAS2      15       0              50K
RFDBACK     17       8              500K
*
```

```
*
* CAPACITORS
C1       17    14      10P
C2       10     9      10P
*
*
* BIASING
VDD       4     0    DC    5
VSS       1     0    DC   -5
VGATE+   21     4    AC   0.0
VGATE-   22     1    AC   0.0
*
*
*   INPUT

VIN       19    0    AC   .02
*
*
* ANALYSES
*
.AC   DEC   200   10K   10MEG
.PRINT AC V(17),V(19)
.PROBE
.END
```

**NOTES
1. This circuit is set up for frequency response determination
2. V(17) and V(19) are the output and input terminals respectively.

```
* C2OA-3
* Based on Ferranti Interdesign type P1 OP-AMP
*
.OPTIONS ITL4=40
.OPTIONS RELTOL=.01
.PARAM A = 1* TRANSISTOR MODELS
**********************************
**NMOS
.MODEL MEDN NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415
+UTRA=0.25 RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10
+VMAX=4.8E4 NEFF=4.0 XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=8.7N
*************************************************
**PMOS
.MODEL MEDP PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30  NFS=5.0E11  CJ=1.05E-4  CJSW=3.0E-10  VMAX=5.0E4
NEFF=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=8.7N
***********************************
*
*
* Circuit Description (A1 POSITION OP-AMP)
*****************************************
M011    2   7   6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M012    2   7   6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M021    9   0   6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M022    9   0   6   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M051    6   5   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M052    6   5   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M061    5   5   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M062    5   5   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M031    3   3   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M041   10   3   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M042   10   3   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M043   10   3   4   21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M071    2   2   1   22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
```

```
M081      9    2    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
M091      3    2    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
M0101    10    9    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
M0102    10    9    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
M0103    10    9    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=180U PS=163U NRD=0.12 NRS=0.25
*************************************
*
* (A2 POSITION OP AMP)
*************************************
M0111    12    7   11    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0112    12    7   11    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0121    14   13   11    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0122    14   13   11    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0151    11   15    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0152    11   15    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0161    15   15    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0162    15   15    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0131    16   16    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0141    17   16    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0142    17   16    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0143    17   16    4    21   MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
```

```
M0171      12    12   1   22   MEDN  L=12.0U  W=24.0U  AD=720P  AS=515P
+PD=108U  PS=91U  NRD=0.25  NRS=0.25
M0181      14    12   1   22   MEDN  L=12.0U  W=24.0U  AD=720P  AS=515P
+PD=180U  PS=163U  NRD=0.12  NRS=0.25
M0191      16    12   1   22   MEDN  L=12.0U  W=24.0U  AD=720P  AS=515P
+PD=180U  PS=163U  NRD=0.12  NRS=0.25
M0201      17    14   1   22   MEDN  L=12.0U  W=24.0U  AD=720P  AS=515P
+PD=180U  PS=163U  NRD=0.12  NRS=0.25
M0202      17    14   1   22   MEDN  L=12.0U  W=24.0U  AD=720P  AS=515P
+PD=180U  PS=163U  NRD=0.12  NRS=0.25
M0203      17    14   1   22   MEDN  L=12.0U  W=24.0U  AD=720P  AS=515P
+PD=180U  PS=163U  NRD=0.12  NRS=0.25
*****************************************
* BIAS VOLTAGES
VDD        4     0    DC     5
VSS        1     0    DC    -5
VGATE+     21    4    AC    0.0
VGATE-     22    1    AC    0.0
*****************************************
* RESISTORS
RBIAS1     5     0          {BIC*50K}
RBIAS2     15    0          {BIC*50K}
R5         13    7          12.5K
RA         13    10   {A*12.5K}
R1         7     23         10K
RFDBACK    17    7          10K
*****************************************
* CAPACITORS
C1         10    9          10P
C2         17    14         10P
*****************************************
* INPUT
VIN        23    0          AC   1
*****************************************
* ANALYSES
.AC DEC 200  10K   10MEG
*.STEP PARAM A 1,11,1
*.TRAN .2US 24US
.PRINT AC VDB(17)
.PROBE
.PROBE VP(17)
.END
*
** NOTE
1. V(17) and V(23) are the output and input terminals
respectively.
```

```
* C2OA-4
* Based on Ferranti Interdesign type P1 OP-AMP
*
.OPTIONS ITL4=40
.OPTIONS RELTOL=.01
.PARAM A = 8
* TRANSISTOR MODELS
*********************************
**NMOS
.MODEL MEDN NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415
+UTRA=0.25 RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10
+VMAX=4.8E4 NEFF=4.0 XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=8.7N
************************************************
**PMOS
.MODEL MEDP PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30    NFS=5.0E11    CJ=1.05E-4    CJSW=3.0E-10    VMAX=5.0E4
NEFF=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=8.7N
**************************************
*
*
* Circuit Description (A1 POSITION OP-AMP)
**************************************
M011     2    7    6    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M012     2    7    6    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M021     9    8    6    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M022     9    8    6    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M051     6    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M052     6    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M061     5    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M062     5    5    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M031     3    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M041    10    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M042    10    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M043    10    3    4    21   MEDP L=12.0U W=60.0U AD=1800P AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M071     2    2    1    22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
```

```
M081      9    2    1    22    MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M091      3    2    1    22    MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0101    10    9    1    22    MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0102    10    9    1    22    MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0103    10    9    1    22    MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
*****************************************
*
* (A2 POSITION OP AMP)
*****************************************
M0111      12    7    11    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0112      12    7    11    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0121      14    13    11    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0122      14    13    11    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0151      11    15    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0152      11    15    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0161      15    15    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0162      15    15    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0131      16    16    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0141      17    16    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0142      17    16    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
M0143      17    16    4    21    MEDP L=12.0U W=60.0U AD=1800P
AS=1290P
+PD=180U PS=163U NRD=0.12 NRS=0.12
```

```
M0171      12   12   1   22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0181      14   12   1   22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0191      16   12   1   22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0201      17   14   1   22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0202      17   14   1   22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
M0203      17   14   1   22   MEDN L=12.0U W=24.0U AD=720P AS=515P
+PD=108U PS=91U NRD=0.25 NRS=0.25
*********************************************
* BIAS VOLTAGES
VDD        4    0    DC    5
VSS        1    0    DC    -5
VGATE+     21   4    AC    0.0
VGATE-     22   1    AC    0.0
VBIAS      8    0    AC    0.0
*****************************************
* RESISTORS
RBIAS1     5    0         50K
RBIAS2     15   0         50K
R6         13   8         12.5K
RA         13   10   {A*12.5K}
R1         7    23        10K
RFDBACK    17   7         10K
*****************************************
* CAPACITORS
C1         10   9         10P
C2         17   14        10P
*****************************************
* INPUTS
VIN        23   0         AC   1
*****************************************
* ANALYSES
.AC DEC 200   10K   10MEG

*.STEP PARAM A 1,11,1
*.TRAN .2US 24US
.PRINT AC VDB(17)
.PROBE
.PROBE VP(17)
.END
*
** NOTE
1. V(17) and V(23) are the output and input terminals
respectively.
```

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